

# Controlling Switch-Reconfigured Antennas Using FPGAs

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## Introduction

Different types of switches such as RF MEMS [1], p-i-n and Schottky diodes [2] have been used to achieve antenna reconfiguration. This paper proposes the reconfiguration of antennas through the use of p-i-n diodes to connect sub-sections to a main antenna section. The activation and deactivation of these p-i-n diodes is controlled through a field programmable gate array (FPGA), which manages the overall antenna configuration under software control. The antenna design, structure, tuning and the FPGA programming is investigated in the present paper. This antenna was fabricated, and the FPGA-controlled p-i-n diodes antenna was tested. The measured results show good agreement with the simulated data.

## Reconfigurable Antenna Structure

The antenna structure is microstrip consisting of a square ground plane, a dielectric substrate with relative dielectric permittivity  $\epsilon_r=4.2$  and height 0.235 cm, and an upper layer of metallic strips (patch). The patch is composed of a main mid-section and four surrounding smaller sections as shown in Fig. 1. The antenna is fed through a 50  $\Omega$  coaxial cable. The antenna dimensions along with the feeding position are shown in Table I.

The variations in configuration are achieved through individually controllable switches, each implemented as a p-i-n diode. Microsemi's GC 4712 GaAs p-i-n diodes are used to connect the small section to the main section as shown in Fig.1. These p-i-n diodes operate up to 18 GHz and are oriented in the  $x$ -direction.

47 pF capacitors are connecting the p-i-n diodes to the main section of the antenna; these capacitors are oriented in the  $y$ -direction and are used to prevent the DC current from crossing into the main section while they allow the RF current to pass through. Quarter wavelength transmission lines designed at 7.7 GHz are used to bias the p-i-n diodes. These  $\lambda/4$  lines are terminated by  $\lambda/4$  radial stubs. Biasing these p-i-n diodes separately allows the connection of the corresponding side sections to the respective mid-section.

To reduce fabrication costs, the biasing lines are etched on copper. These copper lines will resonate at a frequency where the length of the bias lines is approximately  $0.45\lambda_{\text{eff}}$  and at its odd multiples;  $\lambda_{\text{eff}}$  being the effective wavelength at the frequency of operation. In this case these lines resonate around 9 GHz and its odd multiples, which are outside the desired operating band (1-6GHz) of this antenna. The directions of the biasing lines are also optimized to contribute constructively to the radiation pattern of the antenna that is reconfigured.

The antenna achieves multi-frequency resonance tuning which is shown in Fig. 2a. The 4 configurations shown represent an example of the 16 possible configurations achieving frequency change. This shift is noticed at frequencies lower than 3.5 GHz where a lot of wireless communications applications can be found; which improves the practicality of the design. In Fig. 2, a ‘0’ represents the OFF state of a diode and a ‘1’ represents the ON.

A comparison between the *E*-plane cuts of the simulated and measured radiation patterns at 4.875 GHz when all switches are ‘OFF’ is shown in Fig. 2b. The pattern was measured at a resonant frequency common to all the antenna configurations.

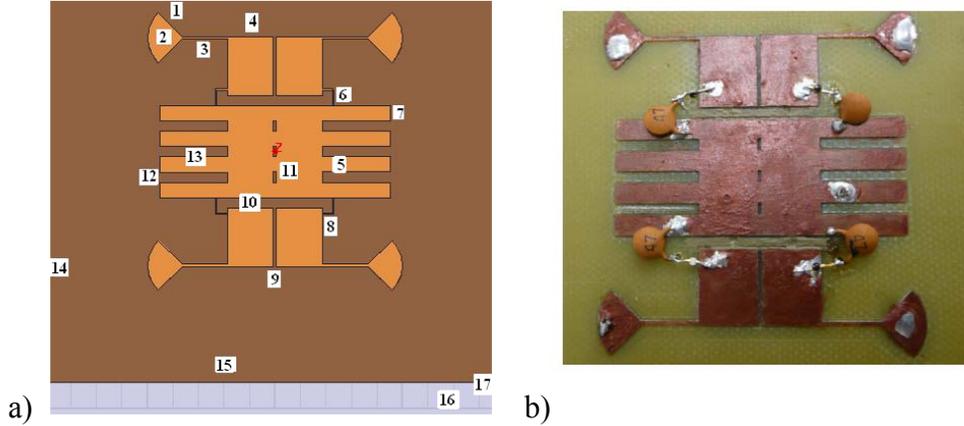


Figure 1. a) Schematic Diagram of the reconfigurable multi-frequency antenna, and b) photo of the fabricated prototype.

TABLE I. ANTENNA DIMENSIONS AND FEEDING LOCATION

Part	Description	Value	Part	Description	Value
1	Radial Stub	6.921mm	9	Outer Patch X Gap	0.6 mm
2	Radial Stub Angle	90°	10	Outer Patch Y Gap	2 mm
3	Quarter Wave T.L. X: 8.959, Y: 0.5mm		11	Main Patch Hole	X:0.6, Y:2mm
4	Outer Patch Width	9mm	12	Main Patch Arm Gap	Y: 2mm
5	Feed Position	X: 12.5, Y: -2.5mm	13	Main Patch Arm X	X:13.2 mm
6	Capacitor	X: 0.25, Y: 3mm	14	Substrate Y	90 mm
7	Main Arm Y	3mm	15	Substrate X	90 mm
8	Diode	X:2, Y:0.25 mm	16	Substrate Dielectric	4.2· $\epsilon_0$
			17	Substrate Height	H: 2.35mm

### Reconfigurable Antenna Measurement and FPGA Control

The fabricated prototype is shown in Fig. 1b. Shorting pins were inserted into 0.75 mm diameter holes drilled at the point of intersection between the p-i-n diodes and the 47 pF capacitors to connect the Microsemi’s GC 4712 GaAs p-i-n diodes to the ground. The VCC is connected to the through pins across holes drilled in the radial stubs. To implement the configuration control infrastructure for this reconfigurable antenna, an FPGA is used to implement a TAP controller as shown in Fig. 3a. The FPGA’s output lines feed the shorting pins to activate and de-activate the p-i-n diodes.

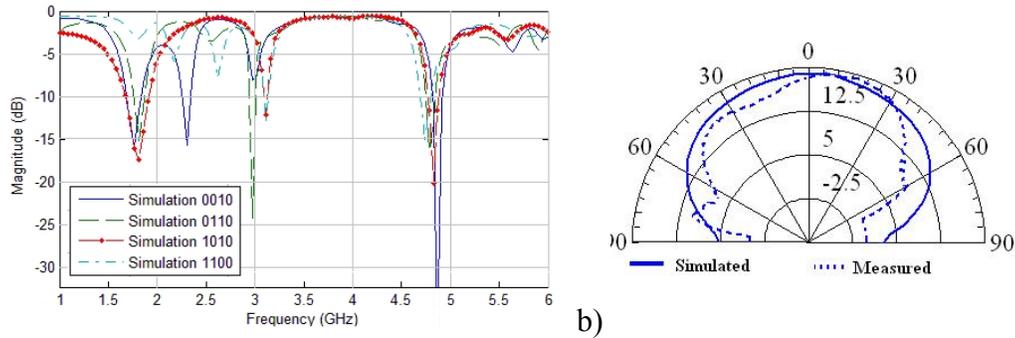


Figure 2. a) Antenna resonance for different diodes states 0-Diode 'OFF', 1- Diode 'ON'. b) Comparison between the *E*-Plane cut of the simulated and measured radiation pattern at 4.875 GHz for all switches 'OFF'

The FPGA implements a Test Access Point (TAP) controller to manage the state of these outputs using a design consistent with the IEEE 1149.1 JTAG standard [3]. A Digilent Spartan 3E board with a Xilinx Spartan XC3S500E FPGA is programmed with the TAP Controller module. A Xilinx Parallel III cable is connected from a parallel port on a Linux PC to the JTAG interface pins on the Spartan 3E board [4]. Four pins on the Spartan 3E board serve as the outputs for driving signals to the diode biasing network. The parallel III cable as well as the board is shown in Fig. 3b.

Antenna reconfiguration is achieved through the following setup: A Linux computer runs the JTAG software, issuing instructions to a Spartan 3E Xilinx FPGA over a Parallel III cable. The TAP controller programmed on the FPGA translates these instructions and asserts the associated signals to bias the p-i-n diodes on the antenna. The FPGA is programmed using VHDL [5]. With one p-i-n diode forward-biased, the RF signal passes from the main patch through the capacitor and that diode to the outer patch.

The measurement and reconfiguration setup used to set and measure individual configurations (of the sixteen possible in this design) is shown in Fig. 4a. A comparison between the simulated and measured  $S_{11}$  results is shown in Fig. 4b for one configuration, demonstrating a reasonable degree of correlation.

### Conclusion

The antenna in this paper is reconfigured using p-i-n diodes as switches. The diodes connect and disconnect four different sections to a main patch to achieve resonance tuning. The control of these p-i-n diodes is achieved through an FPGA implementing a TAP controller compliant with the popular JTAG standard.

The FPGA controlling board constitutes the lower layer of the antenna system. The antenna with the incorporated diodes was designed, fabricated and measured and the control process was achieved with programmed FPGAs

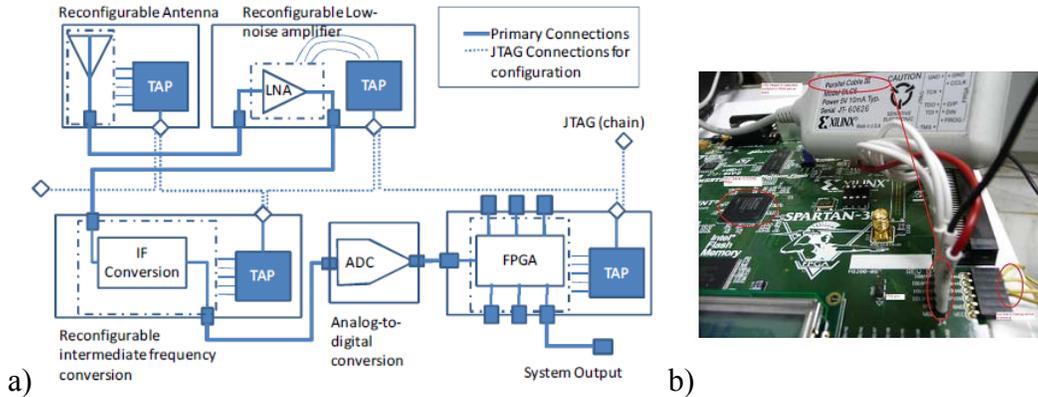


Figure 3. a) Canonical reconfigurable system based on connection of configurable and non-configurable components, controlled by common JTAG scan chain. b) The parallel III cable with FPGA board

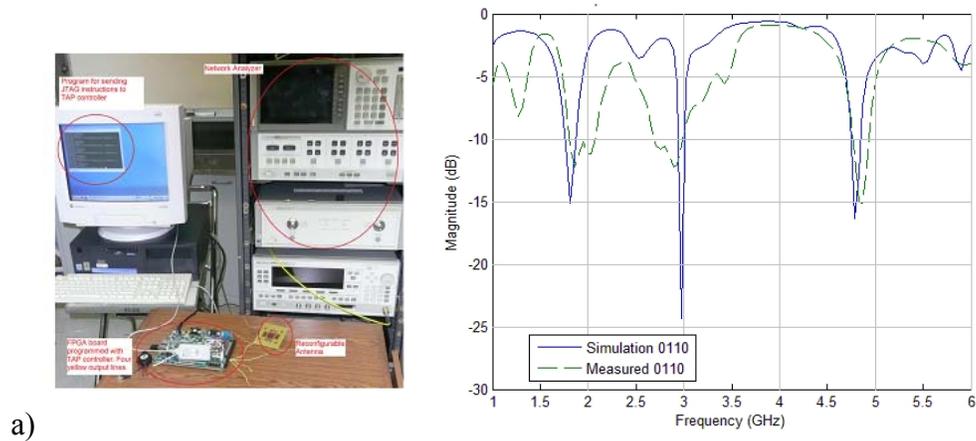


Figure 4. a) Measurement setup and b) measured and simulated  $S_{11}$  for the 0110 case

## References

- [1] D. E. Anagnostou, G. Zheng, M. T. Chryssomallis, J. C. Lyke, G. E. Ponchak, J. Papapolymerou and C. G. Christodoulou, "Design, fabrication and measurements of an RF-MEMS-based self-similar reconfigurable antenna", *IEEE Transactions on Antennas and Propagation*, V.54, I. 2, pt. 1, Feb. 2006, pp. 422-432.
- [2] N.Jin, F.Yang, Y. Rahmat Samii "A Novel Patch Antenna With Switchable Slot (PASS): Dual-Frequency Operation With Reversed Circular Polarizations", *IEEE Transactions on Antennas and Propagation*, Vol. 54, No. 3, pp. 1031-1034, March 2006
- [3] IEEE Standard Test Access Port and Boundary-Scan Architecture, available at: [http://standards.ieee.org/reading/ieee/std\\_public/description/testtech/1149.11990\\_desc.html](http://standards.ieee.org/reading/ieee/std_public/description/testtech/1149.11990_desc.html)
- [4] Spartan-3E FPGA Starter Kit Board User Guide, available at [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug230.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug230.pdf)
- [5] Neil H. E. Weste and D. Harris, CMOS VLSI Design, Pearson Education, Boston, MA, 2005.