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Form 836 (7/06)

Eight Years of MBU Data: What Does It All Mean?

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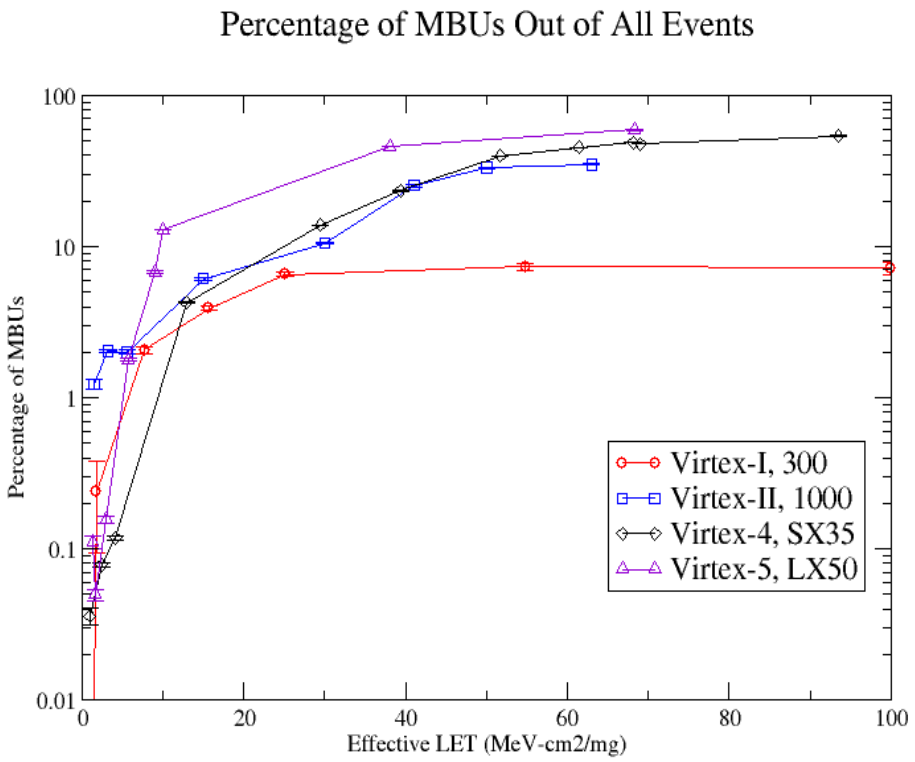
The Standard Message:
Multiple-Bit Upsets in FPGAs Get Worse Each Generation



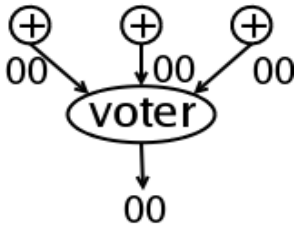
- Over 50% MBUs for V4 and V5 from a normal incidence at highest LETs
- Over 70% MBUs for V5 at a 60° angle in Kr
- What does this mean to spacecraft designers?

Beyond Academics:
What Are the Real Questions?

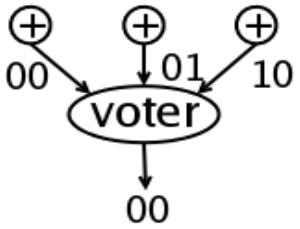
- Each generation has it's improvements and foibles
  - Layout and feature shrink strongly influences MBUs
  - Both have changed greatly over eight years
  - What is the most important information?
- Spacecraft designers need to know:
  - Why should I be concerned?
  - What MBU characteristics should I be concerned about?
  - Can I reliably fly these parts with >70% MBUs?

Why Am I Concerned?

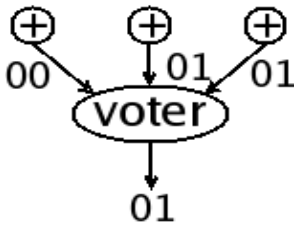
- MBUs break the underlying assumption for TMR'd systems
  - Designer assumes only one error in the system at a time
  - MBUs can manifest as multiple independent errors or span redundant circuit copies (i.e., “domain crossing errors”)



Operating Correctly



Masking Vote



Domain Crossing Error

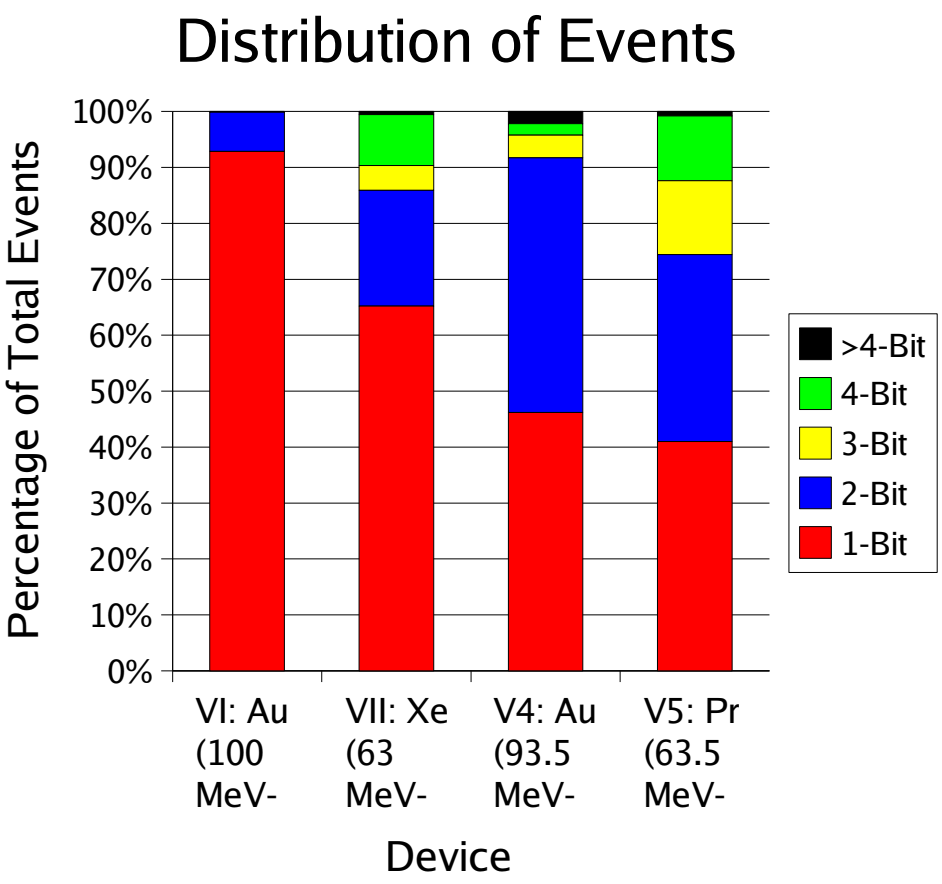
TMR Implications:
How Can I Protect Designs from SBU and MBUs?

- Most SBUs will be fixed with TMR
- Domain crossing errors can be fixed through a combination of TMR and spacing the design properly on the device
  - MBUs, even MIEs, in one domain can be voted out
  - MBUs in two or more domains might or might be voted out, based on whether they are DCEs
- MBUs have a strong proximal connection
  - Domains need to be separated on the device if possible
  - The tools are going to fight you

TMR Implications:
Map and Par for Space Applications

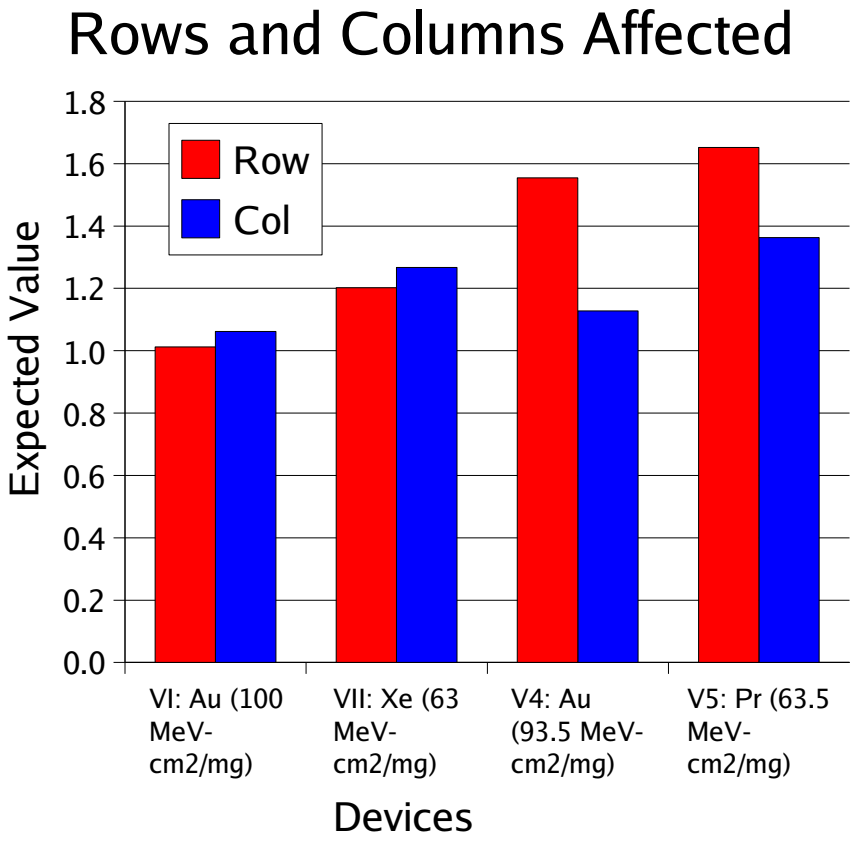
- Synthesis tools that translate circuit description to FPGA programming data attempt to minimize power, execution time by shortening paths
- Synthesis tools are not aware of TMR
  - Redundant circuits placed in proximity, share routing resources
  - MBUs that span LUTs (V4) and LUT/routing network (V5) could span domains
- Lacking control of architecture, synthesis tools need TMR-aware synthesis tools or post-synthesis fixes
  - Rora: post-synthesis fix of routing network

MBUs Characteristics: Distribution of Events



- ~99% of all events are 1- to 4-bit events for all devices
- V4: 1-bit and 2-bit events are equally likely
- V5: 3- and 4-bit events are 25% of all events, larger events less likely than V4

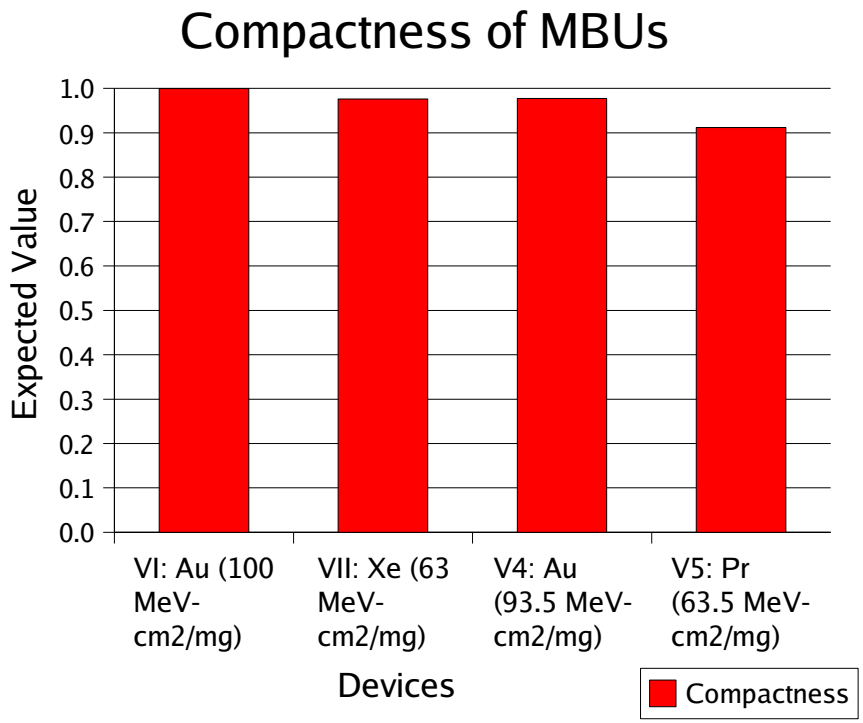
MBUs Characteristics:
Row/Column Coverage



- Redundant copies need to be placed outside of the affected area
- More MBUs ⇒ more rows and cols affected
- Devices appear to be more row adjacent than column adjacent

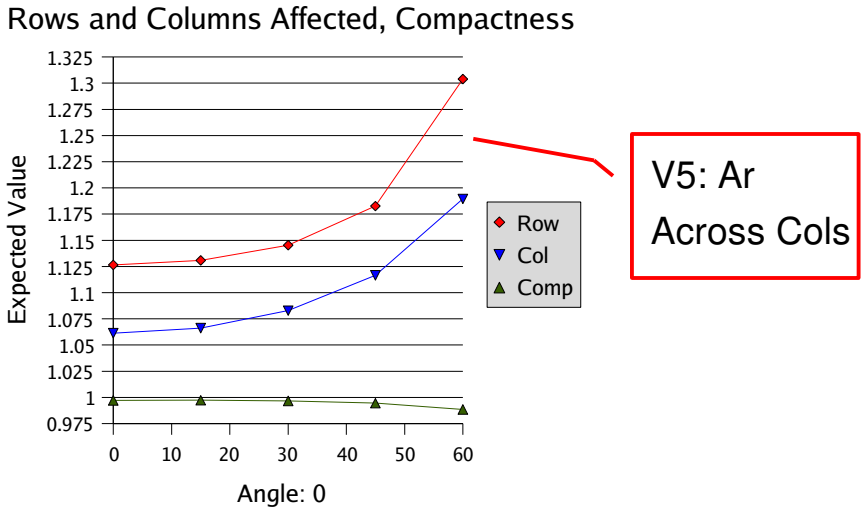
MBUs Characteristics: Compactness

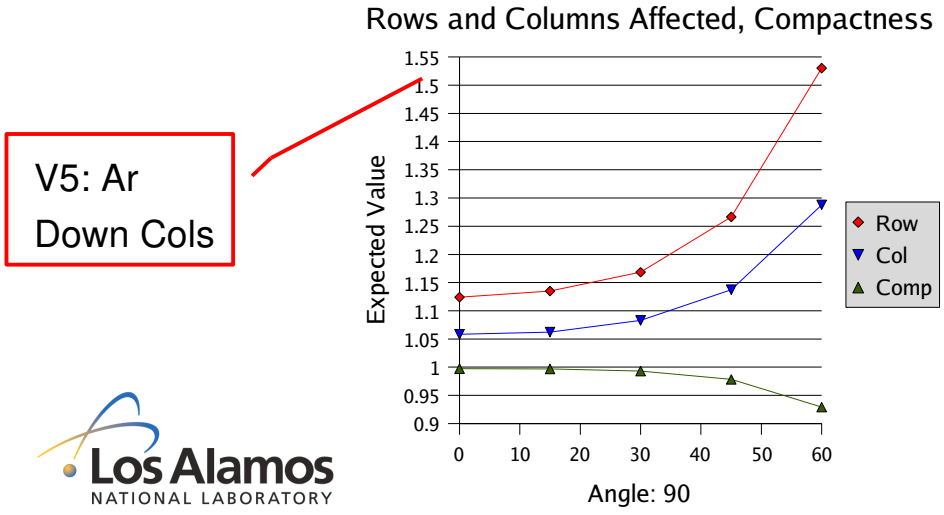
$$compactness = \frac{(S_E)}{(S_{BB})}$$



- Compactness is a measure of how much space MBU takes
- MBUs become less compact each generation: affected area larger than MBUs imply
- V5: Many MBUs involve diagonal components, MBUs lose compactness

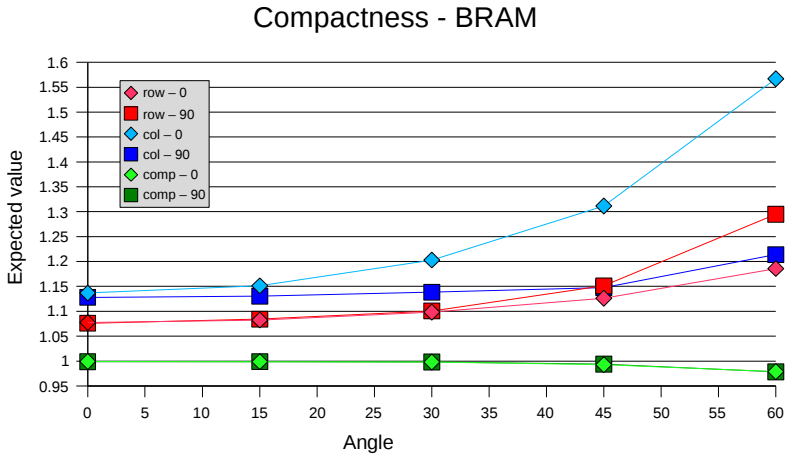
MBUs Characteristics: Angular Effects

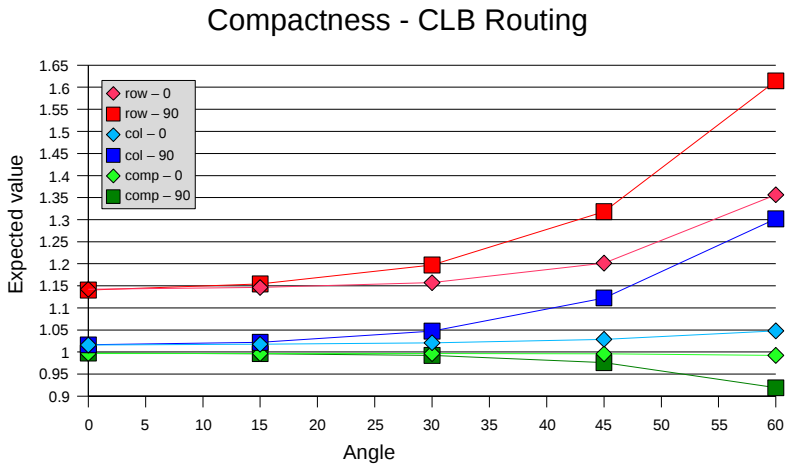




- Strong angular affects
  - More rows and columns affected with angle, compactness decreases
- Different characteristics based on orientation of device in beam
  - Device is row adjacent, strikes down the column maximize effect
- Need to integrate these results for on-orbit rates

MBUs Characteristics:
Angle/Resource Connection





- Need to take the resource differences into account for mitigation
- Difference in orientation response is caused by resources
  - BRAMs are strongly column adjacent
  - CLBs are row adjacent, lose compactness down columns

MBU Characteristics:
CLB Architectural Novelties

- MBUs that span multiple resources are more likely to be domain crossing errors
- VI and VII: MBUs rarely spanned resources
- V4: 10% of the MBUs in the CLB LUT resource span two LUTs
- V5: LUT spanning less common, but MBUs spanning multiple CLB resources (LUTs, routing, state space) more common

TMR Implications:
Fault Injection on VII Test Circuits

- All circuits exhibit MBU DCEs
  - Handful of IOB, BRAMi, and GCLK DCEs
  - Most MBU DCEs are in the CLB routing resources
    - One DCE that crossed from routing to LUT
- Two circuits exhibited SBU DCEs
  - SBU DCEs only occurred in the CLB routing network
  - Rest of resources require MBUs for DCEs?
- Routing resources are congested, entangled
- Initial attempt at determining the probability of a DCE from any possible event is at most 0.5% for VII and 4% for V5

Conclusions

- MBUs do get worse...
  - Angular effects
  - Resource effects
- ...but can be reasonably handled
  - In lieu of architecture changes, change the tools
  - Post-synthesis tools needs to address MBU issues