Xilinx Virtex V Field Programmable Gate Array Dose Rate Upset Investigations

Alonzo Vera[1], Daniel Llamocca[1], Joe Fabula[2], William Kemp[3], Richard Marquez[4], Walter Shedd[4], David Alexander[4]

***Abstract*-- The results of ionizing dose rate experiments on XC5VLX50T FPGAs demonstrate the most susceptible upset mechanism of commercial devices and provide insight into the effectiveness of dose rate hardening of nano-scale technology by using epi substrates.**

I. INTRODUCTION

The Xilinx Virtex V FPGA (Field Programmable Gate Array) family is the present state-of-the-art in commercially available reconfigurable logic devices. Virtex V FPGAs are fabricated in 0.65 nm technology and support clock rates up to 550 MHz, serial I/O (input/output) links up to 3.75 GBPS, and as many as 1200 I/O pins, 330,000 logic cells, and 640 dedicated DSP (digital signal processor) slices. In addition, this family is supported by large offerings of soft IP (intellectual property) to assist the developer in instantiating a variety of designs. These features make the devices extremely attractive to developers of systems with low level radiation requirements.

In the following paper, the authors present the results of ionizing dose rate experiments on the XC5VLX50T FPGA. The experiments were designed to investigate the most susceptible upset mechanism of commercial devices. Previous tests on members of the Xilinx Virtex 4 and Virtex 2Pro families have indicated that the clock was particularly susceptible to upset [1]. Therefore, clock buffering schemes were given primary attention in this work. In addition, the manufacturer made available experimental devices fabricated on two different thicknesses of epitaxial substrates – one typical epi thickness for nano-scale processes and another that was aggressively thinner. The tests were intended to gain insight into the effectiveness of dose rate hardening of nano-scale technology by using epi substrates.

II. TECHNICAL APPROACH

The Virtex V FPGAs are truly systems-on-a-chip, and as such are extremely difficult and expensive to test. The authors' approach has been to divide the effort into a series of tests with each individual test having a clearly defined but limited objective. The Virtex-5 LXT/SXT UG229-V2.0 Prototype platform board available from Xilinx was used for the upset testing reported in this paper. A photograph of the board is shown in Figure 1.

Figure 1. UG229 Virtex-5 LXT Prototype Platform [2]

The device under test was located in the socket shown as item "12" in the photograph. The board used in the dose rate test employed a different socket that did not obscure the part with the socket lid. This particular board was selected because the device under test was isolated from the other active components on the board so they could be shielded from the radiation. The board has independent power terminals for the FPGA core voltage (Vcore), the I/O voltage (Vio), and the auxiliary voltage (Vaux). Other active components on the card were driven from a separate supply terminal. Although direct photocurrent measurements could not be made with this board, the supply currents from each source were monitored after each radiation pulse to check for latch-up. For the tests reported here, all voltages were set at their nominal levels (Vcore = 1.0 volt; Vio = 2.5 volts; Vaux = 2.5 volts).

The board with a XC5VLX50T FPGA was irradiated at the Air Force Research Laboratory Field Emission 705 2-MeV Flash X-ray facility. Dosimetry was based on a PIN diode calibrated against CaF_2 thermo luminescent dosimeters

Manuscript received July 25, 2008.

[1] A. Vera and D. Llamocca are with the University of New Mexico, Dept. Electrical & Computer Engineering, Albuquerque, NM, 87131

[2] J. Fabula is with Xilinx Inc., 5842 N. Camino Del Mar, Tucson, AZ, 85718

[3] W. Kemp is with SES Consultants, Inc., 10701-D Montgomery Blvd NE, Albuquerque, NM 87111

[4] R. Marquez, W. Shedd & D. Alexander are with Air Force Research Lab, 3550 Aberdeen, Kirtland AFB, NM, 87117

(TLDs). The TLDs were exposed behind the lid of one of the commercial packages placed in the board socket.

III. ELECTRICAL CONFIGURATION

Two circuit instantiations were tested in the work reported here. The first circuit was a long shift register chain implemented using all the SRLC32E primitive resources available in the FPGA. This configuration was selected because previous tests on the Virtex IV family had shown the SRL chains and the DCM (Digital Clock Manager) clock to be most susceptible to dose rate upset [1]. Four equally spaced taps were taken off of the shift register and brought out as signals DOUT0 through DOUT3. A 50 MHz clock was used to drive the shift register through an on-chip DCM. The DCM output was provided as an output and monitored as CLKOUT. Outputs DOUT1, DOUT3, CLKOUT, and the PIN diode were monitored on a 500 MHz Tektronix TDS-5054 oscilloscope. All of the digital outputs and the analog waveform of the PIN diode were recorded on a Tektronix TLA 715 logic analyzer/pattern generator. The experimental configuration is illustrated in Fig. 2.

The second circuit configuration used the BRAM (block random access memory) to construct a large FIFO (first –in-first-out) memory. In this configuration a GCB (General Clock Buffer) was used in the first series of test. A second series of tests were performed with the clock buffered by the DCM.

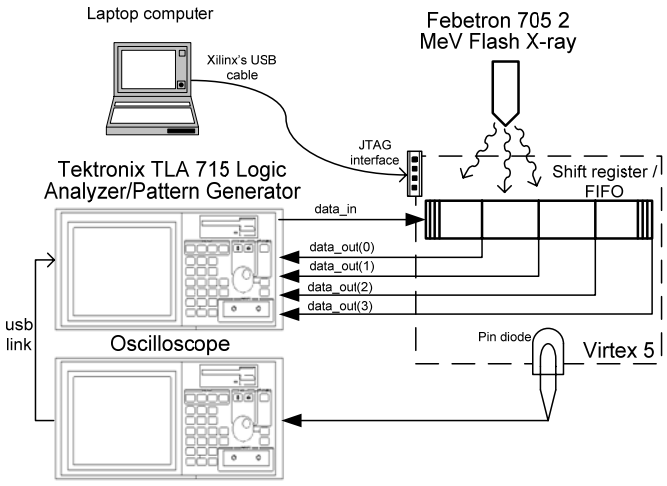

Figure 2. Experimental configuration

IV. EXPERIMENTAL RESULTS

Initial radiation testing was performed on the commercial version of the XC5VLX50T. Figure 3 shows a typical upset response of the first test circuit (SRL32 shift register) as recorded on the oscilloscope. The PIN diode response on channel 4 (magenta) indicates the location of the radiation pulse. No upsets are seen in the shift register data – channels 2 (red) and 3 (green). Although there is no immediate upset in the clock (channel 1, blue) at the radiation pulse, approximately 600 ns after the pulse, the CLKOUT drops out. This loss of the clock can be seen at the very end of the traces in Fig. 3. The full behavior of the DCM clock is shown more clearly in the logic analyzer traces in Figure 4. The CLKOUT trace shows the dropout followed by a subsequent recovery approximately 2μs later. Note that there is no loss of data in the shift register. The register outputs retain their state and commence shifting data out once the clock restarts. As the dose rate was reduced, the drop-out of the clock was eliminated, but the period of the clock changed beginning after the radiation pulse and reverting back to the pre-radiation value approximately 600 ns later. This behavior is shown in Figure 5. Once the threshold was reached where the period broadening appeared, increasing the dose rate by a factor of 1.5 caused the response to transition into the clock drop-out response. Further increasing the dose rate produced longer drop-out durations, and the drop-out occurred closer to the radiation pulse.

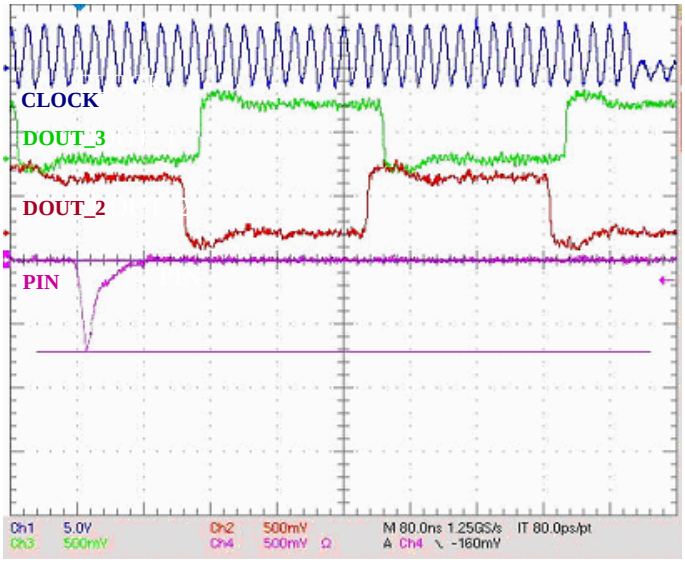

Figure 3. Dose rate response of a commercial XC5VLX50T showing clock drop-out

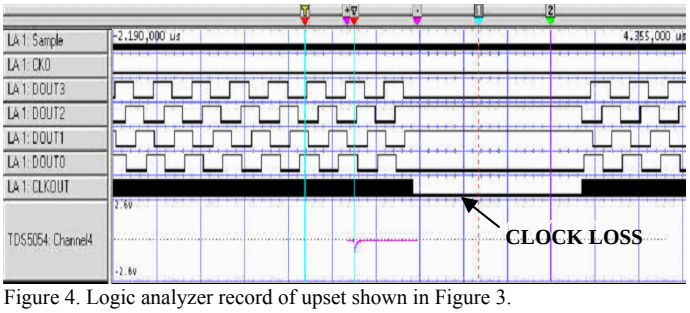

Figure 4. Logic analyzer record of upset shown in Figure 3.

Since the upset in the clock circuitry obscured other upset characteristics and appeared to be associated with the loss of lock in the DLL (Delay Lock Loop) in the DCM, the second test circuit (BRAM-based FIFO) was configured to use only the GCB. The upset characteristic of this circuit is shown in Fig. 6, which was the minimum upset threshold measured for the BRAM/FIFO.

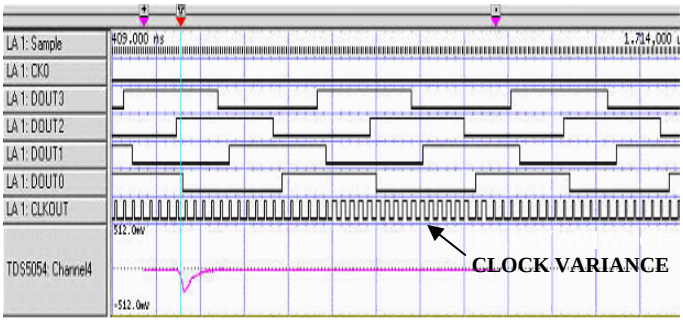

Figure 5. Dose rate response of commercial XC5VLX50T showing a variance in the clock cycle

Note that the single clock upset occurred very soon after the radiation pulse. The logic analyzer data for the same shot is shown in Fig. 7 and shows no indication of upset occurring at a later time.

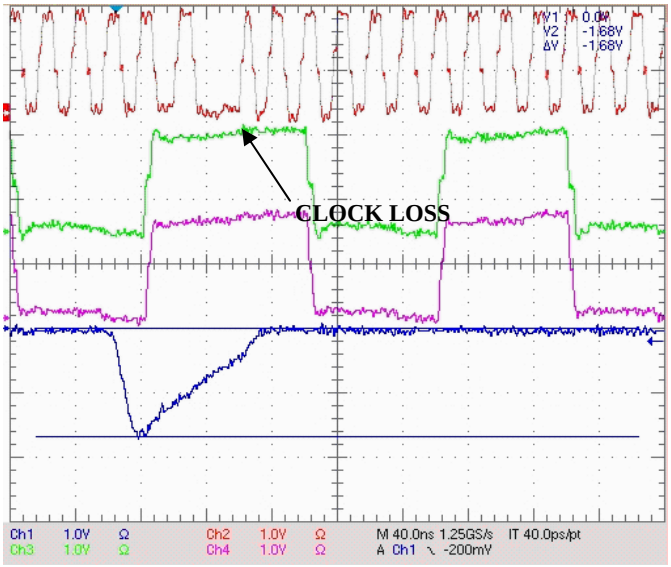

Figure 6. Minimum upset characteristic for BRAM/FIFO using the GCB for clock buffering.

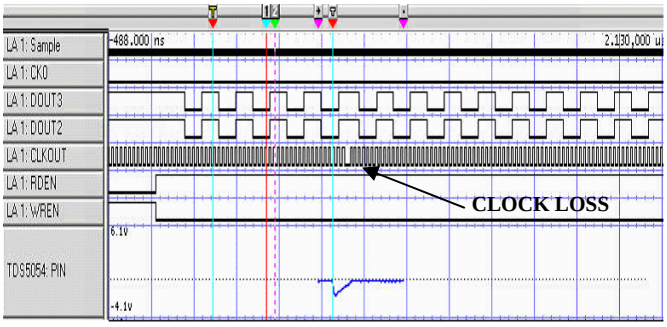

Figure 7. Logic analyzer record for BRAM/FIFO minimum upset characteristic for the BRAM/FIFO.

To verify that the DCM/DLL was responsible for the latent upset observed previously, the configuration of the BRAM/FIFO was changed so that the clock was routed first into the GCB and then into the DCM/DLL buffer. The results are shown in Fig. 8 and Fig. 9.

Both the oscilloscope trace and the logic analyzer trace show the loss of a clock pulse near the radiation pulse. This response is characteristic of GCB upsets. The logic analyzer trace shows a subsequent drop out of clock for several cycles, which is characteristic of loss of lock in the DCM/DLL.

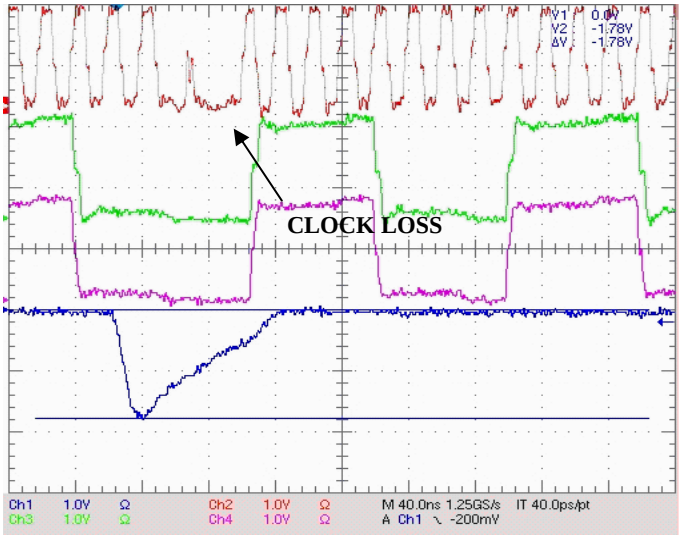

Figure 8. BRAM/FIFO lowest upset threshold showing characteristic GCB upset

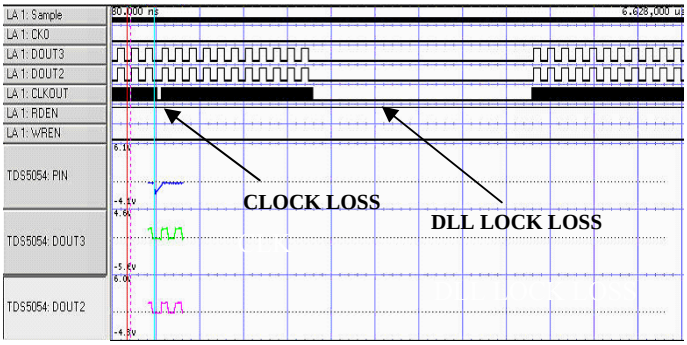

Figure 9. BRAM/FIFO lowest upset threshold showing latent upset characteristic of DCM/DLL.

V. Results of Epitaxial Thickness Investigation

For both the shift register and BRAM/FIFO instantiations, the upset test results of the XC5VLX50T samples fabricated on epitaxial substrates showed the same qualitative behavior as the non-epitaxial commercial parts. The latent loss of lock in the DCM/DLL was observed as the initial upset characteristic in both the typical and aggressive epi, just as it was in the commercial device. The only change was the quantitative onset of upset. Both epitaxial devices experienced clock drop-out if the dose rate was high enough. Similarly, the BRAM/FIFO upsets were qualitatively the same in the commercial and the two epi devices. Although, either of the two epi thicknesses increased the upset threshold, the aggressive epi thickness was much more effective for both the shift register and BRAM/FIFO instantiations.

A comparison of the thresholds for the maximum no-upset dose rate for the three versions of the FPGA is shown in Figure 10 for both instantiations. The epi substrate that is

typically used with 65nm technology only improved the upset threshold by a factor of 1.33 for the shift register instantiation. The more aggressive, thin epi improved the threshold by a factor of 8.2.

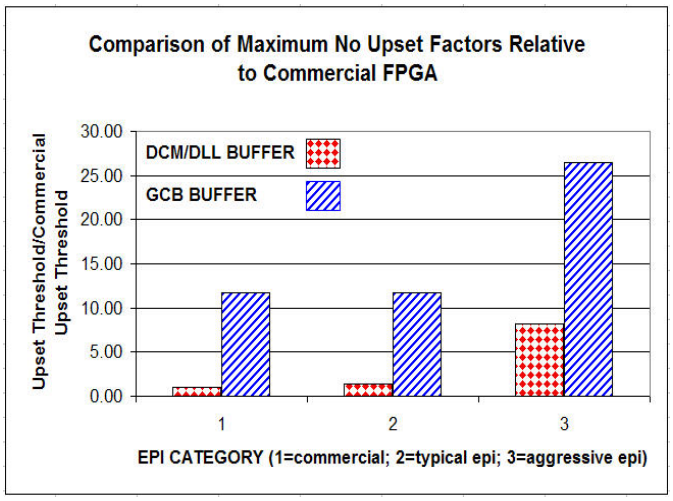

Figure 10. Comparison of maximum no-upset threshold for a commercial bulk silicon substrate and two experimental epi thicknesses

VI. SUMMARY

Two important results were identified in these tests. First, experimenters should be careful when performing dose rate testing on complex circuits to record significant portions of the data stream following the dose rate pulse to ensure that an upset does not occur downstream from the actual pulse. This is particularly the case for microcircuits using complex delay lock loop (DLL) clock synchronization schemes such as those in the Xilinx DCM. The observed response was probably due to the loss of lock in the DLL. However, the observation of this phenomenon required the acquisition of data at long times after the pulse with a logic analyzer. If the observations were limited to typical oscilloscope recording times of 200 ns to 500 ns, the upset could easily be missed with the result of attributing erroneously higher upset thresholds to the device.

Secondly, the effectiveness of the two epi thicknesses was shown to be much different. The typical thickness only slightly increased the upset threshold; while the aggressive thickness increased the threshold by nearly an order of magnitude or more for circuits using clock buffers implemented with the GCB. However, the aggressive epi material had some adverse effects on the performance of the devices (i.e., increased leakage currents). Thus, the traditional techniques of dose rate hardening through the use of epitaxial substrates must be carefully applied to balance hardening effectiveness against impacting device performance.

VII. REFERENCES

[1] Alonzo Vera, et al., Dose Rate Upset Investigations on the Xilinx Virtex IV Field Programmable Gate Arrays, Radiation Effects Data Workshop, July, 2007.

[2] Virtex-5 LXT/SXT/FXT FPGA Prototype Platform User Guide, Xilinx, UG229.