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Affordable Rad-Hard – An Impossible Dream?

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ABSTRACT

Affordable electronics and radiation-hardened electronics have often been mutually exclusive terms. Recent activities at the Air Force Research Laboratory (AFRL) and other government organizations are focused on vastly improving the availability and affordability of high-performance rad-hard electronics to put them into the price range of small satellites. The projects include the development of an advanced FPGA, structured ASICs, 16-Mbit SRAMs, and hardened versions of commercial devices such as a Texas Instrument 1394 chip set.

INTRODUCTION

Satellites, even small satellites, are expensive in terms of labor hours expended, price of purchased modules, and launch costs. Failure of even the most humble piecepart (diode, transistor, etc.) can cause the mission to fail and waste all of the resources expended to field it. Consequently, great care and discipline are required in selecting the pieceparts that make up the electronics packages that acquire, process, and communicate data and control the satellite. The parts must survive launch and function in the thermal and radiation environment of space for the duration of the mission.

A radiation-hardened part is always the desirable choice for a satellite application even though its performance (throughput, power dissipation, etc.) is lower and its price is higher when compared to a commercial device. The added expense of testing a commercial microcircuit to ensure adequate radiation hardness and reliability can quickly exceed the purchase price of a rad-hard part. Design schemes such as TMR (triple modular redundancy) to mitigate SEE (single event effects) in commercial parts, greatly complicate the design of the hardware and software, driving up cost and extending development time. In cases where the commercial microcircuit is susceptible to latch-up in the space environment, on-board latch-up monitoring and recovery functions must be added to the system design. Such provisions not only increase complexity and cost, but also call into question the reliability of parts that may experience latch-up even for a short time.

Despite the benefits of using radiation-hardened parts for space system reliability and survivability, their performance has seriously lagged that of commercially-available electronics. Furthermore, the variety of available rad-hard electronics is far less rich than commercial offerings. Finally, the price and delivery time for rad-hard products have often been prohibitive for small satellites on a tight budget and short schedule. As a result, small satellite programs are tempted to accept much greater risk than they would like and to fly commercial parts with only superficial testing.

NEW CONCEPTS IN HARDENING MICROELECTRONICS

Improving the availability and cost of state-of-the-art radiation-hardened microcircuits is clearly a worthy objective. Achieving this objective requires a vision of future satellite parts requirements and an appreciation of the impact on radiation hardness and hardening techniques as the semiconductor industry follows its roadmap of shrinking feature size, advanced materials, and new processes.

The authors' vision of the future of satellite systems foresees continued pressure in the following areas: (1) flat or tightly constrained piecepart budgets, (2) significantly reduced development times, (3) decreased power allocations to drive down weight and reduce launch costs, (4) increased on-board processing and data storage to reduce downlink bottlenecks, and (5) standardization of interfaces. In the area of data processing functions, we expect system designers will respond to these pressures by changing the technology mix they use to satisfy

processing requirements. We anticipate they will choose a mix where roughly 50% of the functionality is instantiated in FPGAs (field programmable gate arrays), 25% in S-ASICs (Structured Application Specific Integrated Circuits), 15% in catalog ICs, and 10% in full custom ASICs. The rationale behind those choices is to enable more of the functionality to be instantiated in configurable microcircuits (FPGAs and S-ASICs) and hardened versions of commercial catalog parts. In our vision, the goal is to architect the system to restrict full-custom ASICs to those few critical functions requiring the most extreme performance. This approach will enable system designers to achieve the performance they need while minimizing the high NRE costs associated with ASIC design and mask fabrication in nano-scale (i.e., 90 nm and below) technologies. However, these expectations require that advanced electronic technologies be enhanced to increase their radiation hardness while reducing non-recurring costs and assuring availability.

In the following sections, we briefly describe some of the programs that are in progress and provide opportunities to achieve radiation-hardened data processing at an affordable cost.

Radiation-Hardened Volatile FPGA Development

The SIRF (SEU-Immune Reconfigurable FPGA) program is an effort sponsored by AFRL to develop a radiation-hardened version of the Xilinx Virtex 5 commercial FPGA, specifically, the XQR5VFX130. The characteristics of the device are listed in Table 1.

Table 1: SIRF Device Characteristics

Function	Size
Logic cells	131,072
6-input Look-up Tables (LUT)	81,920
Distributed RAM (Kbits)	1,580
36 Kbit BRAM Blocks	301
BRAM (Kbits)	10,836
Clock Management Tiles	6
DSP48E Slices	320
GTX Channels	20
PowerPC 440 Blocks	2
PCI Expres Endpoint Blocks	3
10/100/1000 Ethernet MACs	6
Select I/O	840
Rocket I/O Channels	20

The physical organization of the SIRF chip is shown in Figure 1.

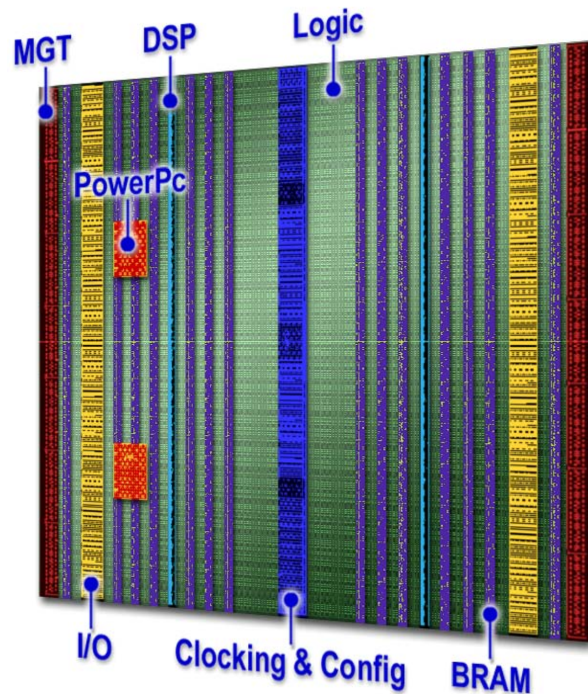

Figure 1: Physical layout of the SIRF chip

Note that the functions of the SIRF Virtex 5 are segregated into columns in the layout. This columnar architecture facilitates the implementation of hardening-by-design (HBD) approaches. Size increases required to accommodate HBD techniques are constrained to the vertical dimension, leaving the lateral dimension unchanged and not affecting the lateral routing resources. This permits relatively easy scaling of the size of the FPGA dimensions to maintain required functionality even though there is an increase in the physical dimensions of the HBD cells.

The SIRF Virtex 5 is fabricated with 65nm, nano-scale technology with 12 layers of metallization. It is the state-of-the-art commercial FPGA technology that achieves 50% to 70% of the performance (i.e., clock frequency, gate density, and power) of a custom ASIC fabricated in the same technology. However, the design costs are 70% to 80% less than the costs of a custom ASIC; the design tools are 99% less than ASIC tools (standard Xilinx commercial tools are used for the enhanced SIRF FPGA); qualification and procurement costs are 100% less than an ASIC (i.e., $0); and schedule lead time is 66% to 75% less than an ASIC. AFRL estimates that for an equivalent 1 Mgate design, a standard cell ASIC development would required 2 years and $10M, whereas an FPGA implementation would require 6 months and $2M.

The primary hardening effort is being applied to limit single event effects (SEE). The goal of the project is to eliminate SEL (single event latch-up), reduce SEU (single event upset) in the data path circuitry to 10^{-2}

errors per device day and SEU in the configuration memory to 10^{-4} errors per device day. This is being achieved by use of space and time redundancy and error correcting techniques in the data memory, flip flops, and registers. Special electrical and layout designs are used to harden the configuration memory while the state machines have been redesigned to eliminate SEFI (single event functional interrupts). The PowerPC 440 (PPC 440) and the Rocket I/O are macro-cells (special purpose circuits) that are often used in the Virtex 5. Hardening analyses have been conducted on those macro-cells, but the elements will not be hardened in the initial development effort.

Two proof-of-concept test chips have been completed to date, and the first prototype of the full rad-hard Virtex 5 is scheduled to complete fabrication and testing by the end of calendar year 2008. The final product is scheduled to be available for purchase in the first quarter of 2010.

Radiation-Hardened Structured ASIC Development

The radiation-hardened structured ASIC (S-ASIC) program is being sponsored by AFRL in an enhanced SBIR (Small Business Innovative Research) program. The program team is led by Microelectronics Research and Development Corp (Micro-RDC), and includes ViASIC, Inc., Adsantec, Sandia Technologies, and Aeroflex. The program is based on a structured ASIC concept developed by ViASIC and employs the primitive cell shown in Figure 2.

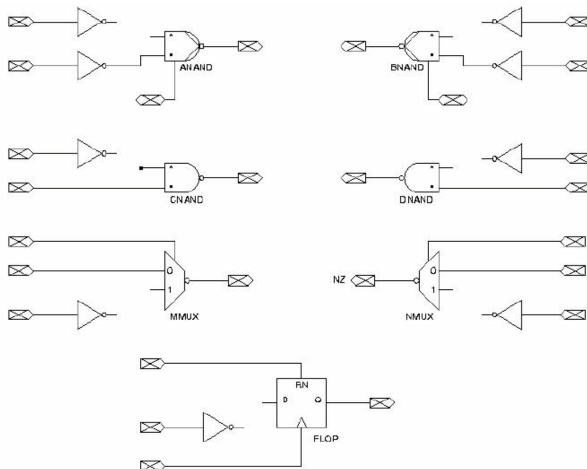

Figure 2. Structured ASIC Primitive Cell

The primitive is combined with 8 bits of memory to form a tile which is replicated in an array to form the structured ASIC (Figure 3 is a block diagram of a 2x2 tile array). Once the S-ASIC wafers are produced, a customer's design (i.e., the instantiation) only requires one mask layer to "configure" the devices rather than the full set of mask layers (typically 24 or more) needed to produce a custom ASIC. This results in a substantial reduction in mask cost. Also, the wafers will be pre-processed and held just prior to the instantiation step, thereby reducing fabrication time. For the final step, any traditional IC (integrated circuit) design that is compatible with the S-ASIC can be developed using existing automated IC design tools then be instantiated in the array using the ViaPath® tool from ViASIC.

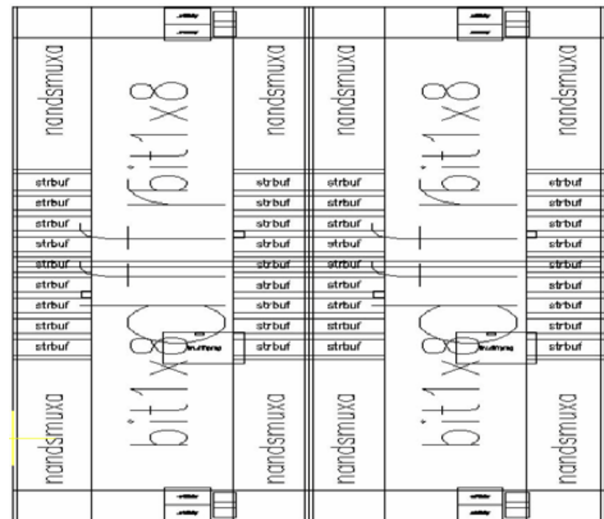

Figure 3. Tile of 2x2 Logic Cells and Memory

In addition to the S-ASIC fabric, several hard macro-cells have been designed to be integrated into the fabric. These include: ROM blocks, SRAM blocks, phase lock loop, SERDES, and LVDS I/O. The full mask reticle has been divided into several different sizes of S-ASIC, each with different resources. Figure 4 depicts the arrangement of the die on the reticle. Area has been set aside on the reticle for a Reliability Test Coupon (RTC). The RTC includes test structures to evaluate the intrinsic reliability and radiation hardness of the process, and includes structures for: electromigration, via integrity, stress voiding, gate oxide integrity, interlevel dielectric integrity, hot carrier effects, negative bias instability effects, and total dose hardness monitoring. These structures are arranged for probe testing at the wafer level. There is also a segment dedicated to lot qualification testing for evaluating extrinsic reliability and radiation hardness. These devices have been included specifically to support qualification and lot acceptance testing.

As with the SIRF, the S-ASIC uses HBD techniques to ensure reliable operation in space environments. Specifically, some of the HBD techniques used include:

- Edgeless NMOS transistors to eliminate source-drain leakage,
- Intervening P-plus channel stops to eliminate field oxide leakage and latch-up,
- Spatial and temporal redundant latches to mitigate SEU (single event upset) and SETs (single event transients), and

- Robust metallization with frequent N-well and P-well contacts to mitigate secondary photocurrent effects.

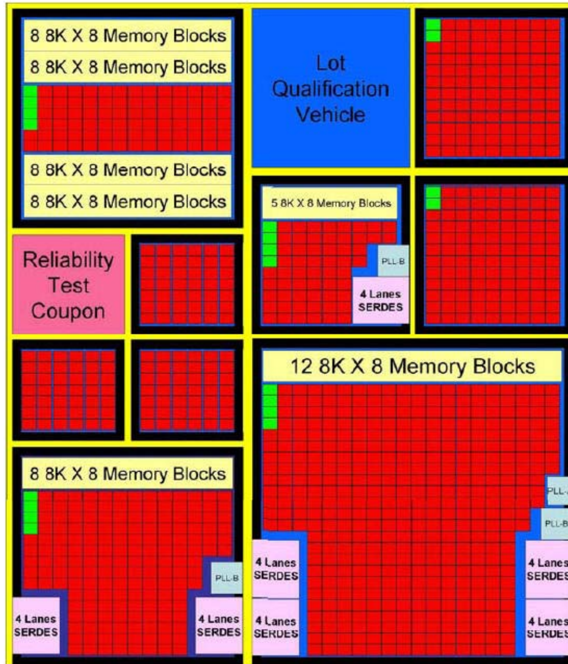

Figure 4. Reticle Floor plan for S-ASIC

The characteristics of each of the die in the S-ASIC reticle are listed in Table 2. The reticle will be fabricated in the IBM 9LP process, a low-power, 90 nm technology with 12 layers of metal. The current schedule is for the first full design to be released in October 2008 with evaluation devices available in February 2009. Full qualification is expected by September 2009. Once the full mask set has been verified, subsequent lots will require only one mask layer to be fabricated, all other layers will be reused. Schedules for lot submissions and pricing for the various die sizes will be determined by the development team. Mr. Steve Philpy (719-531-0805) at Micro-RDC is the point of contact for further information.

Minimally Invasive Processing Modifications for Standard Product Hardening

Modern microcircuit fabrication processes rely on precisely controlled implant doses and energies with thermal activation to determine performance characteristics. In some cases, these processes can be modified to improve the radiation tolerance of the resulting microcircuits. If these modifications are relatively minor, high volume foundries may be willing to incorporate them into their recipes. Programs to demonstrate the effectiveness of these minimally invasive techniques have been supported by AFRL and other agencies through SBIR efforts with Silicon Space Technology, Inc. (SST). Thus far, these programs have resulted in a 16 Mbit SRAM with initial standby current less than 250 μA that remains less than 2 mA after 1 Mrad of total ionizing dose radiation. The part is latch-up free and incorporates error detection and correction and scrubbing for SEE mitigation.

In addition to the SRAM, the SST minimally invasive process has been applied to Texas Instruments 1394 Firewire chip set (physical layer and PCI interface), providing a 4X improvement in total-dose performance and elimination of latch-up. Additional efforts are underway for similar hardening of the Texas Instruments TMS320VC33 and TMS320C2812 digital signal processors. Qualification of the 16 Mbit SRAM is expected to be completed in the first quarter of calendar year 2009. Qualification dates for the other devices have not been determined at the time of this article. Mr. Jon Gwin (210-822-9706) of Silicon Space Technology is the point of contact for the availability of these parts.

HARDENED BY DESIGN LIBRARY FOR AFFORDABLE ASICS

Development of a standard cell ASIC is often too expensive for small satellite programs. However, the Defense Threat Reduction Agency has sponsored a program with Boeing Solid State Electronics Development (SSED) Group to develop a radiation-hardened-by-design ASIC library for IBM 90 nm

Table 2. S-ASIC Die Characteristics

Die Size	Total Pads	Pwr/GND	CMOS User IO	SERDES	PLL	Block SRAM	Distributed DP SRAM	Equivalent Logic Gates	SERDES LVDS*	PLL	VROM
3 x 3	172	60	96	0	0	None	~86K Bits	~126k	No	No	None
5 x 5 A	276	112	158	0	0	None	~217K Bits	~318K	No	No	256K Bits
5 x 5 B	276	92	128	28	18	5 Blocks 8K X 8	~125K Bits	~183K	Yes (4 Lanes)	Yes	512K Bits
7 x 7 A	410	114	192	56	18	7 Blocks 8K X 8	~356K Bits	~522K	Yes (8 Lanes)	Yes	512K Bits
7 x 7 B	410	154	248	0	0	28 Blocks 8K X 8	~164K Bits	~240K	No	No	512K Bits
10 x 10	604	152	328	112	31	8 Blocks 8K X 8	~850K Bits	~1.2M	Yes (16 Lanes)	Yes	512K Bits

* LVDS IO is only available if not using the SERDES lane(s).

9SF technology[1]. By using the library for small volume, multi-project lots through MOSIS, custom ASICs can be developed for reasonable costs. The library is the property of the U.S. Government and is available for use by DoD (Department of Defense) approved organizations through Boeing SSED. The point of contact is Dr. Warren Snapp (253-773-5722).

The library contains over 1014 cells and has parameterized options for speed, power, and radiation hardness. The electrical, functional, and radiation characterization of the library is complete. The library provides EDA (electronic design automation) views for the major software tools, and the library models have been validated. Table 3 lists the data included in the library to support specific design steps and tools and some of the validation test chips are shown in Figure 5. The library has been used for multiple microcircuit designs at Boeing. It includes robust cells for SEU mitigation, while work is ongoing for additional characterization of single event transient effects.

Table 3. Support Data for Boeing Radiation-Hardened Library

Development Step	Data included
Synthesis	• Liberty Format Files (.lib) • Synopsys Data Base Files (.db)
Simulation	• Verilog simulation models • VHDL VITAL simulation models • Cadence schematics
Placement & Routing	• Cell physical geometry • Cell frame views • Cell timing views • Cell power views • Technology file
Verification	• Cell SPICE netlist • Verification decks version
Support data	• Cell datasheets • Models & Design rules version

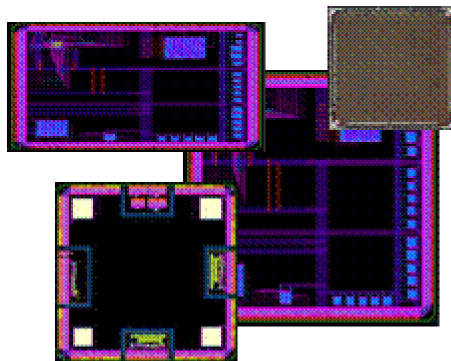

Figure 5. Validation Test Chips for Boeing Radiation-Hardened by Design Library

The design cost of developing an ASIC depends on the design complexity and the experience of the design team. Similarly, the packaging, testing, and qualification efforts depend on the size and intricacy of the device. However, for relatively small ASICs the cost of fabrication in a multiproject lot can be quite reasonable. For example, a 16 mm^2 die for the IBM 9SF process can be fabricated through MOSIS for $125,000 for 40 die. This could be a viable cost structure for a project needing a very specialized function.

SUMMARY

Radiation-hardened microelectronics to support space applications have historically been extremely expensive with long acquisition times. However, several initiatives to reduce cost and improve availability have been reviewed in this paper. Configurable devices such as FPGAs offer the opportunity to provide design flexibility while realizing the benefits of volume production of a commodity part. Structured ASICs provide both design flexibility and significant reduction in fabrication costs and development cycles. Similarly, the use of minimally invasive process modifications may make radiation-hardened versions of commercial catalog parts available to the space community. The advantages of catalog parts in terms of documentation, development tools, and experienced engineering infrastructure can result in significant overall savings. Finally, the availability of a well characterized radiation-hardened library for an advanced technology node opens opportunities for small volume custom ASIC designs fabricated through multi-project lots. Together these approaches offer the promise of affordable, radiation-hardened microelectronics to future space systems.

REFERENCES

1. Cohn, L. M., "DTRA Radiation Hardened Microelectronics Program: RH 90nm Technology Development Program," 2008 Fault Tolerant Space-borne Computing Workshop.