Qualification & Reliability Monitoring for Small Quantity ASIC Populations

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***Abstract*— The authors present a discussion of the issues and an approach for qualification and reliability monitoring for small quantity ASICs used in long lifetime applications. Special attention is given to issues associated with sub-100 nm technologies and the unique challenges posed by new materials and processes.**

Keywords-ASICs, lifetime, qualification, reliability

I. INTRODUCTION

The availability of nano-scale ASICs (application specific integrated circuits) offers major opportunities for electronic systems including: higher performance, lower power per function and greater density per function. Unfortunately, these opportunities are accompanied by significantly higher design and fabrication costs and potential erosion in the expected lifetime of the ASICs due to the use of new materials and processing techniques. Those organizations requiring large volumes of ASICs for their applications often reach agreements with the foundry to participate in the foundry's reliability monitoring programs which are based on thorough process qualification procedures to determine dominant failure mechanisms and excellent surveillance programs to ensure that those mechanisms remain under control. Such agreements can be extremely effective in maintaining the required lifetime for products employing very advanced technologies. However, there are numerous applications, which can significantly benefit from nano-scale technologies but require only small quantities of ASICs.

By their very nature, systems with highest reliability requirements often field very few units. Those units may function continuously in locations which are difficult to access and may be required to operate at elevated temperatures and in other environmental conditions that can reduce lifetime. To reduce the cost of small quantities of advanced ASICs, there has been great interest in the use of concepts such as multi-project wafer (MPW) lots, where the cost of a lot is amortized over designs from multiple customers, and structured ASICs (S-ASICs), where the underlayers are standard designs and personalization is implemented with only a few (1 to 3) mask layers. Since these concepts result in only a few wafer lots per year, it may not be cost effective for the foundry to provide the full support of their reliability monitoring program to customers with a small number of infrequently processed lots. Although the small quantity ASICs clearly benefit from the foundry's process qualification and continuous reliability monitoring, the data required to demonstrate the required mission lifetime to qualifying agencies are often unavailable.

The following material presents the results of efforts to support qualification of small quantity ASIC lots by incorporating reliability monitoring test structures as part of the reticle set used to process either multi-project lots or structured ASICs. These techniques have been applied to 180 nm, 130 nm, and 90 nm technologies.

II. STANDARD RELIABILITY TEST COUPON

The objective of a standard reliability test coupon (RTC) is to provide a set of intrinsic reliability monitoring structures for the physical mechanisms that may limit the operational life of ASICs fabricated in a target technology. These mechanisms include: electromigration for each metal layer, stress voiding, via and contact integrity, interlevel dielectric integrity, line-to-line metal extrusion, hot carrier injection as a function of oxide thickness and layout geometry (nmos and pmos), bias temperature instability as a function of oxide thickness (nmos and pmos), and thin oxide effects (dielectric breakdown as a function of area, gate periphery, and field edge periphery). Several of the structures for electromigration, extrusion monitoring, and bias temperature instability incorporate polysilicon heaters to facilitate wafer probe measurements at temperature. Otherwise, the structures are consistent with those widely reported in the literature, but sized to be consistent with the critical dimensions of the target process.

As illustrated in Figure 1, the RTC is laid out for 2x10 probe pads on a NIST standard spacing. For an MPW lot, the RTC is incorporated in each reticle exposure as shown in Figure 2 for a 200 mm wafer providing 54 sites for reliability evaluation. The RTC measurements are most easily made at wafer probe on the undiced wafer. For MPW lots, all of the participants must agree to have the wafer probed before dicing. The concept is based on sharing the cost of the RTC fabrication and testing among the participants in the MPW. The RTC for a 90 nm technology is 25 mm^2. The cost of fabrication is $185,000 and the testing cost is approximately $75,000. Typically, the costs are apportioned among the participants proportionally to the percentage of the reticle area taken by their die. As new technology nodes become available for MPWs the RTC can be retargeted for the smaller critical dimensions for around $25,000. The infrastructure for probes and test software remains essentially the same.

The data taken from wafer probe are used in a variety of ways. For example, the electromigration data are used to establish a correlation between the process design rules and the extrapolated lifetime. In the case of Metal 1 in a 90 nm process, the extrapolated test data indicate a first fail at 31 years for a minimum line width and the maximum current density allowed by the design rules. Thus, the design rules are quite robust for applications with long mission life requirements.

However, in the case of NBTI, the data indicate that for a junction temperature of 90°C and a change in threshold voltage of 50 mV, the projected lifetime is approximately 10 years. While this is more than adequate for most commercial devices, high reliability applications that operate at elevated temperatures must modify their designs to accommodate a larger V_T shift if they are to support mission lifetimes of 15 to 20 years.

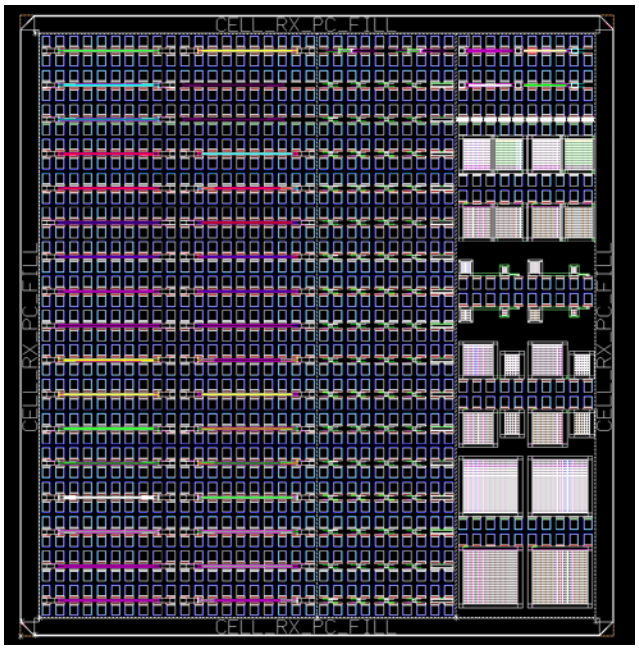

Figure 1. Reliability test coupon layout

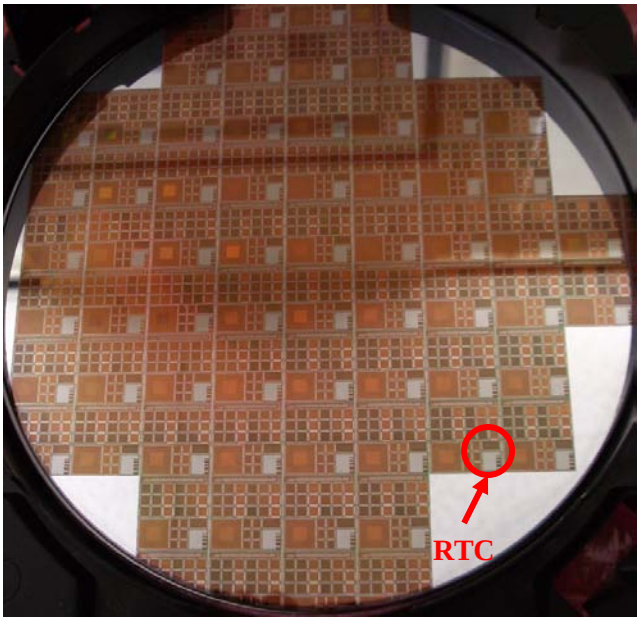

Figure 2. RTC incorporated on an MPW wafer

III. QUALIFICATION WITH THE RTC

While the RTC is effective in monitoring intrinsic reliability and evaluating the adequacy of design rules for extended lifetime missions, it can also be used to support formal qualification of microcircuits used in high reliability applications. The S-ASIC, whose reticle layout is shown in Figure 3, is the most complete example of such a new qualification approach. The reticle layout includes the RTC

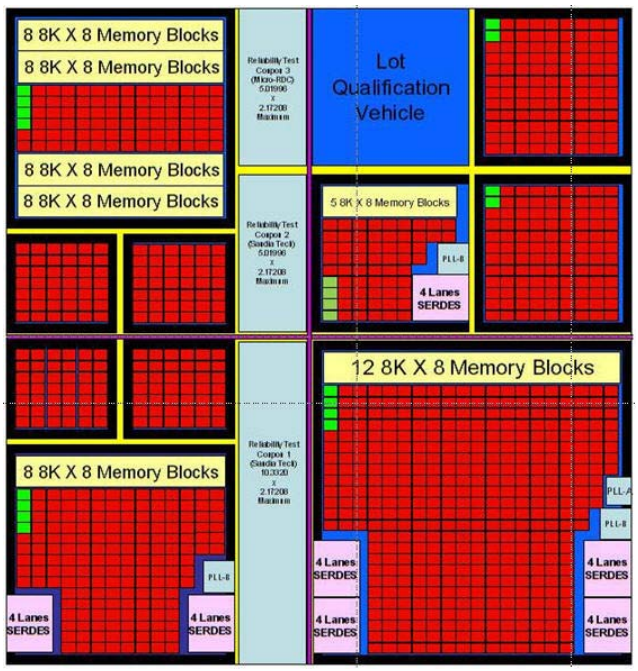

Figure 3. Structured ASIC reticle layout

(light blue) reformatted to extend the entire length of the reticle. In addition to the structures noted previously, it includes logic chains to evaluate propagation delay and setup/hold time.

The remaining die on the reticle are various sizes of the S-ASIC each of which can receive a different personalization. Thus, the reticle becomes an MPW in which participants can select the fabric size and macro types that fit their application. Qualification is performed under Mil-Prf-38535 with the RTC providing intrinsic reliability data and structures for monitoring response to environments such as high temperature. One of the die (dark blue) has been designated the LQV (lot qualification vehicle). Its personalization includes all of the primitives in the S-ASIC fabric as well as all macros (SERDES, PLL, block memory, and ROM) available to the designer on the other die.

To achieve qualification, three lots of the S-ASIC are run with intrinsic reliability data taken on the RTC for each lot. The data are used to establish a reliability baseline in evaluation of future lots for major changes caused by process modifications. Samples from of the LQV from each lot are packaged in high rel ceramic flat packs and subjected to full type A through D screening. A sample of 100 screened parts is then subjected to 4000 hours of accelerated life test. Once qualification is achieved, the LQV serves as a standard burn-in circuit to monitor extrinsic reliability.

IV. Conclusion

An approach has been presented for monitoring reliability and supporting qualification of MPWs and S-ASICs fabricated in small quantities in advanced technology foundries. In each case, a significant amount of silicon space has been devoted to monitoring structures for both extrinsic and intrinsic reliability. However, this may be a small price to pay for assuring reliable parts for applications that require only a small number of devices to operate over extended lifetimes.