MITIGATION TECHNIQUES FOR SINGLE EVENT INDUCED CHARGE SHARING IN A 90 NM BULK CMOS PROCESS

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PURPOSE

Mitigation techniques to reduce the increased SEU cross-section associated with charge sharing in a 90 nm DICE latch are proposed. The increased error cross-section is caused by heavy ion angular strikes depending on the directionality of the ion vector, thereby exacerbating charge sharing among multiple circuit nodes. The use of nodal separation as a mitigation technique shows an order of magnitude decrease on upset cross-section compared to a conventional layout and the use of guard-rings show no noticeable effect on upset cross-section.

Keywords—charge sharing, Dual Interlocked Cell (DICE) latch, guard-rings, heavy-ion, nodal separation, single event circuit characterization, soft error cross-section.

INTRODUCTION

Decreasing technology feature size has resulted in higher packing densities, reduced nodal charge, and reduced device spacing. These features can result in radiation-induced charge collection (the impetus for soft errors) at multiple nodes due to a single incident ion (i.e., charge sharing [1]–[4]). Many different design approaches to mitigate soft errors - such as Triple Mode Redundancy (TMR) [5], temporal latch [6], or Dual Interlocked Cell (DICE) [7] - are based on redundancy assumptions requiring that an incident single-event (SE) ion affects only one circuit node. This assumption is valid for technologies where an ion strike results in charge collection on a single node within the circuit. However, in deep-submicron technologies, this isolation assumption is not valid, and charge sharing between multiple nodes leads to increased susceptibility of hardened circuit designs as shown by Olson *et al.* [2] and Amusan *et al.* [4]. Recent work has also shown a significant dependence of upset cross-sections and LET thresholds on the directionality of the impinging ion vectors due to charge sharing among circuit nodes as seen in Fig. 1 [8]. The directionality of the incident ion vectors is illustrated in Fig. 2, in which *North-to-South* (*N-S*) vectors traverse *orthogonal* to power rails, and *West-to-East* (*W-E*) vectors traverse *parallel* to the power rails.

In this paper, a Radiation-Hardened-By-Design (RHBD) latch array with different implementations of mitigation techniques has been fabricated in a commercial 90 nm bulk CMOS process and the resulting reduced error cross-sections due to heavy-ion exposure is presented. Mitigation schemes are specifically aimed at reducing the directional dependence of soft-error cross-section. The results quantify the effectiveness of layout mitigation schemes in decreasing the hardened latch susceptibility to charge sharing resulting from angular strikes in deep-submicron technologies.

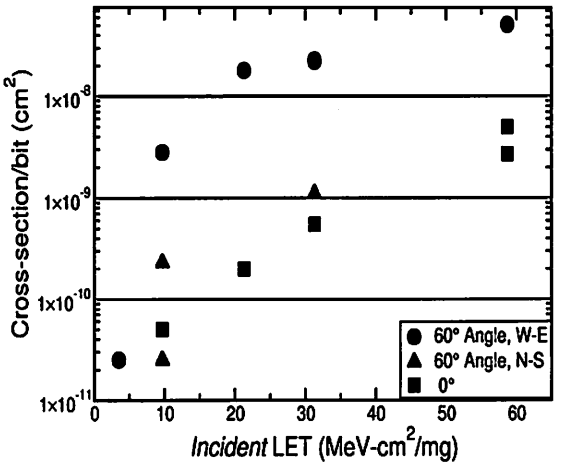

Fig. 1. Heavy-ion data showing a significant dependence of upset cross-sections and LET thresholds on the orientation of the circuit layout for angular SEE circuit characterization [8]

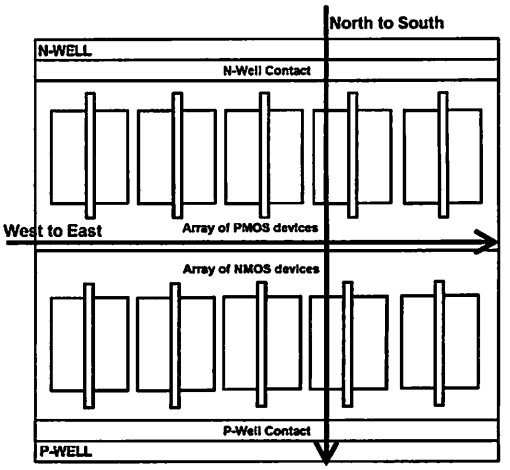

Fig. 2. *North-to-South* (*N-S*) vectors traverse *orthogonal* to power rails, *West-to-East* (*W-E*) vectors traverse *parallel* to the power rails [8].

CHARGE SHARING

The vulnerability of hardened circuit designs to charge sharing was first theorized by Velazco *et al.* [1]. Recent work has shown parasitic bipolar amplification to be a major charge collection effect for PMOS to PMOS charge sharing, whereas for NMOS to NMOS charge sharing, diffusion is the main charge collection mechanism [9]. Olson *et al* have also shown parasitic bipolar amplification to be acute for PMOS transistors in a twin-well bulk CMOS process with p-substrate [10]. The n-well potential collapse from an angular ion strike for PMOS to PMOS charge sharing can be as much as 5 μm

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from the strike entry point as shown in Fig. 3 [11] and can lead to increased charge collection on multiple PMOS transistors placed within that distance. Hence, redundancy based circuit hardening designs are susceptible to charge sharing and this is a major reliability issue. Spacing or separating the sensitive (critical) nodes helps mitigate this phenomenon [9].

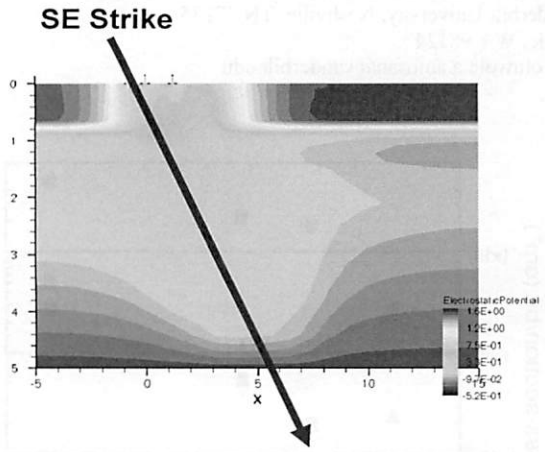

Fig. 3. N-well potential collapse of 4.5 µm - 5 µm from penetration point due to angled strikes; increases charge collection on multiple PMOS transistors [11].

EXPERIMENT

Heavy-ion experiments were conducted at the Lawrence Berkeley National Laboratory on a soft-error-hardened DICE latch. The DICE latch design is an interlocked latch using two storage nodes for each bit to provide information redundancy [7]. As a result, it is considered virtually immune to an upset when a single storage node is perturbed. However, the DICE latch does possess identifiable sensitive node pairs that can upset with simultaneous perturbations on two storage nodes [4]. Mitigation of simultaneous charge collection between sensitive node pairs increases tolerance to single-event soft errors.

Three different DICE layout topologies were considered in the study of sub-100 nm charge sharing induced soft error effects:

1) Layout design without any mitigation technique (i.e., no regard to the location of the sensitive pairs) - NORMAL
2) Mitigation through layout spacing with a minimum 2 µm nodal separation of all sensitive pairs - WOGR (With-Out Guard-Ring)
3) Mitigation through layout spacing with 2 µm nodal separation of the sensitive pairs and in addition placing guard-bands (i.e., contacted well region on all four sides of the transistor) around one of the devices that make up a sensitive pair - WGR (With Guard-Ring)

The 2 µm nodal separation was chosen based on simulation results presented by Amusan *et al.* [9] which show that charge sharing between devices is significantly reduced for a nodal separation of 2 µm. These topologies were designed to investigate directional sensitivity and examine the effectiveness of layout mitigation techniques. The DICE latches were implemented in a shift register fashion with 511 stages and fabricated in a commercial 90 nm bulk CMOS technology.

The ions used were Argon, Copper, Krypton, and Xenon with LET ranging from 9.74 to 58.6 MeV·cm^2/mg. The lower LET range tested represents energies typical of neutron-generated particles [4], [12]. The angles used for exposure were 0° and 60° from normal. The direction of the angled incident ions (i.e., 60°) was varied from *orthogonal* to the power rail (i.e., *North-to-South*) to *parallel* to the power rail (i.e., *West-to-East*) as indicated in Fig. 2. Multiple input data patterns were tested at each ion exposure.

RESULTS

The data in Fig. 4 shows results comparable to previously presented data (Fig. 1. [8]) when no mitigation scheme is employed. Results show that DICE latches are more sensitive to W-E angular single-event strikes compared to the Normal and N-S angular SE strikes. The increase in upset cross-section can be attributed to an increase in multiple node charge collection for sensitive pairs in the same well [9] (i.e., PMOS transistors in n-well and NMOS transistors in p-well) as the strike vectors traverse parallel to the power rails (Fig. 2) affecting multiple sensitive nodes. The effect of the angular ion-strike can be related to terrestrial radiation such as the secondary neutron reaction products which can create multiple ion-tracks with higher energies than the incident neutron [4] and alpha radiation which can deposit charge at very oblique angles [12].

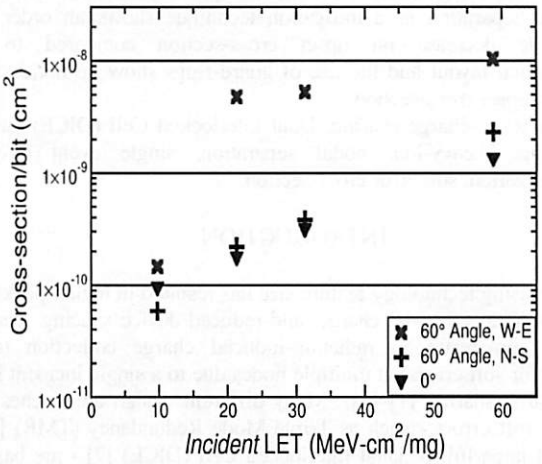

Fig. 4. Heavy-ion data for the NORMAL layout shows an order of magnitude increase in upset cross-section for the 60° W-E strikes in comparison to the 60° N-S and 0° strikes.

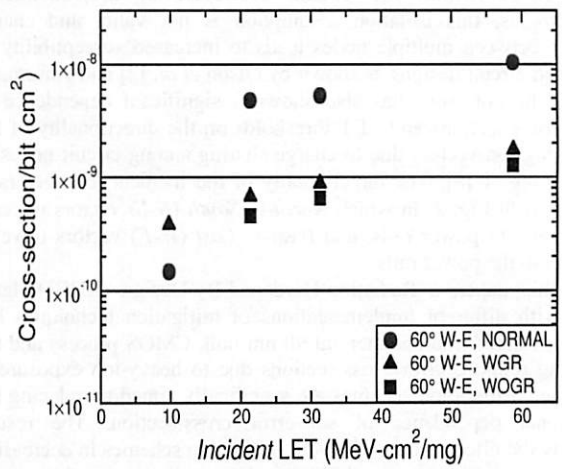

Fig. 5. Evaluation of the 60° W-E data for the three different layout topologies shows an order of magnitude decrease in upset cross-section for the WGR and WOGR layouts in comparison to the NORMAL layout.

The data in Fig. 5 shows a comparison of the three different layout topologies and the effectiveness of the layout mitigation techniques in reducing the order of magnitude increase in upset

cross-section from that seen in Fig. 1 and Fig. 4 for 60° W-E angular strikes. The results show that nodal separation of the sensitive pairs (WOGR layout) is an effective measure in mitigating the directional sensitivity. The resulting cross-section from the 3rd layout topology (WGR layout) which included nodal separation and guard-rings around one of the sensitive pairs is comparable to the WOGR layout. This shows that the guard-ring does not add any appreciable hardness improvement to the DICE circuit.

3D-TCAD Analysis

Using 3D TCAD models calibrated to the match the electrical characteristics of the commercial 90 nm process, charge sharing simulations were conducted to examine the effects of nodal separation and guard-rings on reducing the angular effects of charge sharing.

The 1st set of 3D TCAD mixed-mode simulation was to examine the effect of angular strikes on charge sharing. Simulations were conducted for two NMOS devices simulated in the OFF state (i.e., Gate LOW, Source LOW, Drain HIGH) and two PMOS devices in which both devices were simulated in the OFF state (i.e., Gate High, Source High, Drain LOW - PMOS devices) as illustrated in Fig. 6. The devices were included in a 5-string inverter chain with the rest of the circuit in compact models of the commercial 90 nm process. The struck device is defined as the *active* device, and charge sharing device in proximity to the struck device is defined as the *passive* device. A spacing of 140 nm was used between the active device and passive device, and simulations were conducted for normal hit and 60° angular hit. For the 60° hit, the strike was angled towards the passive device for a worst-case scenario and in all simulations the Drain of the active device was struck.

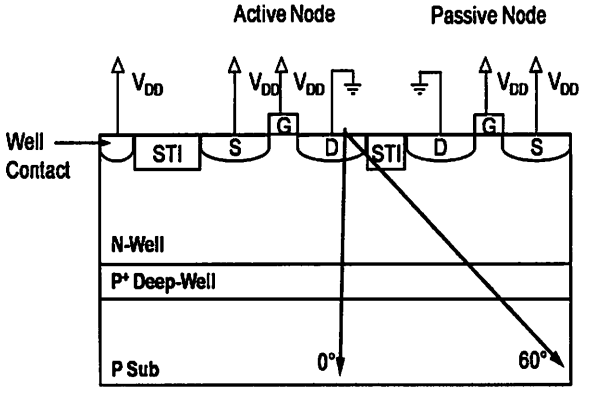

Fig. 6. Illustration of the normal and 60° hits for the PMOS charge sharing setup.

Result in Fig. 7(a) shows the significant increase in charge collection for passive NMOS device for 60° angled strikes in comparison to a normal strike. The increase in the passive NMOS device charge collection for the 60° angled hit is due to the increased ion track length associated with the angled strike traversing underneath the passive NMOS device, thereby increasing the diffusion charge collection on the passive NMOS device [9]. For passive PMOS device, Fig. 7(b) shows the increase in charge collection for the 60° angled hit in comparison to the normal hit. This is due to the collapse of the n-well potential around the ion track traversing directly underneath the passive PMOS device, thereby increasing the parasitic bipolar amplification of SE currents for the passive PMOS device [2], [4], [8]. This increase in passive NMOS/PMOS device charge collection for 60° angled strikes illustrate the order of magnitude increase in upset cross-section for 60° W-E angled strikes shown in Fig. 1 and Fig. 4.

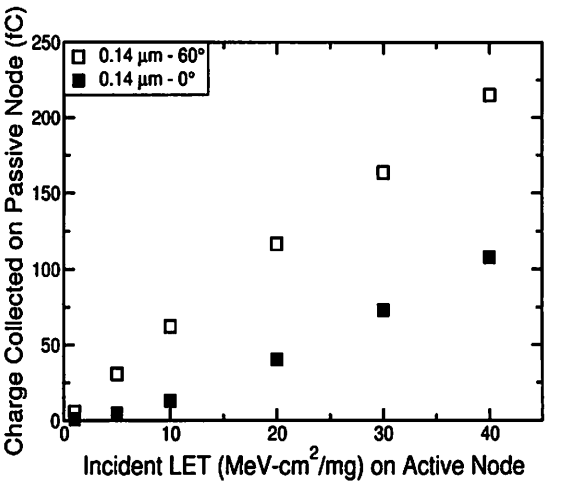

Fig. 7(a). Passive NMOS device charge collection shows a significant increase for 60° angled hit in comparison to a normal hit.

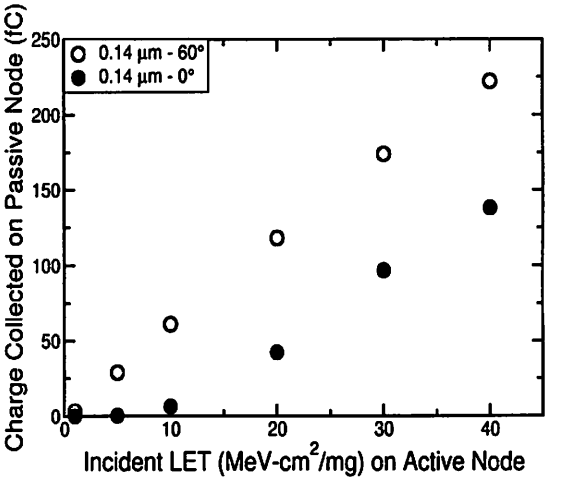

Fig. 7(b). Passive NMOS device charge collection shows a significant increase for 60° angled hit in comparison to a normal hit.

The next set of simulations was to examine the use of guard-rings in mitigating the charge sharing effect. Guard-rings are used as a SE mitigation technique, as they provide additional well-taps to help reduce the well potential collapse required to turn-on the parasitic bipolar transistor [3], [10]. The illustration in Fig. 8 shows the placement of the guard-ring around the passive PMOS device (similar setup for NMOS charge sharing setup).

The result in Fig. 9(a) shows that the guard-ring has no significant effect in reducing the passive NMOS device charge collection. The main reason for this is that the main charge collection for NMOS charge sharing is by charge diffusion [9]. The guard-ring is more effective in reducing the amount of charge collected for the passive PMOS device for both normal and 60° angled hit as seen in Fig. 9(b). The guard-ring helps maintain the n-well potential around the passive PMOS device, thereby limiting the parasitic bipolar amplification of SE related currents. However, the guard-ring does not eliminate charge collection for the passive PMOS device, especially for angled strikes as seen in Fig. 9(b). Furthermore, the guard-ring is ineffective for passive NMOS device charge collection, hence, the insignificance in reducing the upset cross-section (i.e., comparison between WGR vs. WOGR) as seen in Fig. 5.

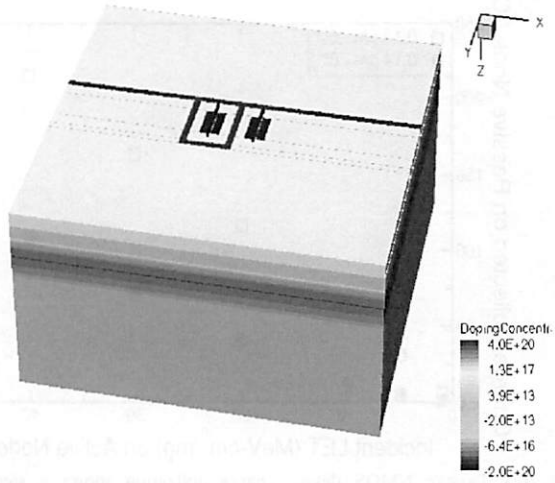

Fig. 8. 3D TCAD structure shows the placement of a guard-ring structure around the passive PMOS device.

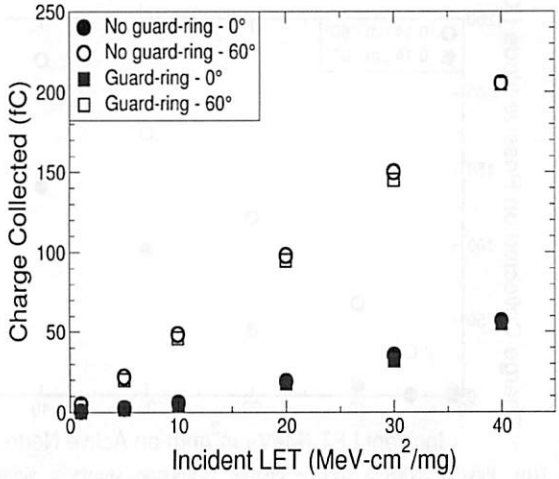

Fig. 9(a). The use of guard-ring has no effects in reducing the passive NMOS device charge collection.

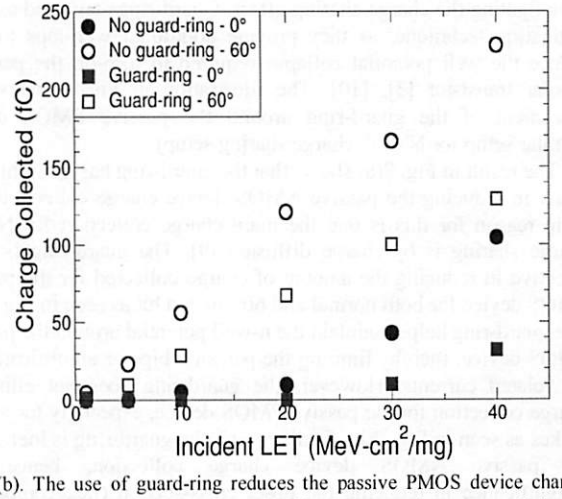

Fig. 9(b). The use of guard-ring reduces the passive PMOS device charge collection for both normal and 60° angled hit. However, the amount of charge collected is still significant and can cause an upset in deep-submicron technologies.

CONCLUSION

This work demonstrates the effectiveness of layout mitigating techniques in reducing the soft-error cross-section (due to charge sharing) in the presence of directional sensitivity in a hardened latch design. The increased charge sharing for transistors in the same well for angular ion strikes depends on the directionality of the strike. Mitigation schemes proposed show that the DICE latch and other redundancy based designs can achieve improved SE hardness by physically separating the sensitive pairs in the layout of the circuit. Another common hardening technique (use of guard-rings) that was used for this design shows no noticeable improvement, due to its inability to overcome parasitic bipolar amplification for PMOS transistors and its ineffectiveness in reducing the charge collection on NMOS transistors.

ACKNOWLEDGEMENTS

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