A Very High Sensitivity RF Pulse Profile Measurement System

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Abstract—A technique for characterizing the pulse profile of a radio-frequency (RF) amplifier over a very wide power range under fast-pulsing conditions is presented. A pulse-modulated transmitter is used to drive a device under test (DUT) with a phase-coded signal that allows for an increased measurement range beyond standard techniques. A measurement receiver that samples points on the output pulse power profile and performs the necessary signal processing and coherent pulse integration, improving the detectability of low-power signals, is described. The measurement technique is applied to two sample amplifiers under fast-pulsing conditions with a pulsewidth of 250 ns at 3-GHz carrier frequency. A full measurement range of greater than 160 dB is achieved, extending the current state of the art in pulse-profiling techniques.

Index Terms—Dynamic range, measurement, modulation, power amplifiers, pulse measurements, transmitters.

I. INTRODUCTION

In typical communication and radar systems, the transmitter is operated in either a continuous wave (CW) or a pulsed mode, where the transmitter is periodically turned on for a portion of time. These systems commonly use a power amplifier in the transmitter to raise the power level of the transmitted signal to a value that is sufficient to meet system sensitivity requirements. In high-dynamic-range systems, the power amplifier pulse must turn off at a rate that is compatible with the system noise floor at the receive time. If the pulse repetition frequency (PRF) is low, then there is a long period of time for energy to dissipate [1], [2]. However, in some high-performance communication systems, the system requirements drive the PRF to be in the megahertz range, and the amount of time between successive transmit and receive gates can be measured in nanoseconds, particularly in systems with a relatively high duty factor (DF).

Some high-dynamic-range systems may be sensitive to signals that are more than 120 dB below the transmit power level [3], [4]. Undesired energy can remain in the system at the time the receiver turns on if the rate of decay of the transmitted energy is not sufficiently high. This residual correlated energy can cause serious system consequences, such as a reduced operational range or a drastic increase in bit error rate due to the increased noise level. Pulsed amplifiers based on field-effect transistor (FET) technologies, such as metal–semiconductor FETs, pseudomorphic high-electron mobility transistors (pHEMTs), or heterojunction FETs, can experience turn-on/off problems arising from gate or drain lag [5], [6].

It is useful in high-dynamic-range systems to characterize the output power of the amplifier pulse versus time, which is referred to as “pulse power profile” in this work. A pictorial view of a sample pulse power profile is shown in Fig. 1.

Traditionally, pulse characterization is performed in the time domain using either a crystal/diode detector or a peak power meter. These techniques allow one to measure the rise and fall times of an RF pulse but do not give insight into the pulse profile over the range required in highly sensitive systems. A simple square-law diode detector is capable of resolving the rise/fall times of an RF pulse but do not give insight into the pulse profile over the range required in highly sensitive systems. A simple square-law diode detector is capable of resolving the rise/fall times of fast-pulsed signals, but the dynamic range is typically limited to less than 30 dB [7]. A peak power meter is commonly used to measure pulsed signals, and a dynamic range of 50–80 dB is achievable with commercial state-of-the-art equipment. However, the video bandwidth in these systems is limited, so that the capability of measuring very fast pulse-modulated signals is degraded. Traditional vector network analyzers (VNAs) offer impressive dynamic ranges of more than 150 dB but have previously been limited to CW measurements. The latest VNA products from industry leaders include options to allow pulse profile measurements with a dynamic range of 70–80 dB for the pulsewidths of interest and a time resolution on the order of 10 ns [8], [9].

However, the previously mentioned techniques do not provide enough dynamic range or sufficient time resolution to measure the full pulse profile for high-dynamic-range fast pulse-mode systems. This work aims to address this critical need by presenting a technique for measurement of the full pulse profile for high-dynamic-range fast pulse-mode systems.
The technique proposed is similar to pulse integration used in radar systems [10]. In pulsed radar systems, multiple returns from a target are either coherently or incoherently combined to increase the detectability of the target. If the combination of pulses is performed before the detection step, where the phase information from the returns is retained, then the process is called predetection integration or coherent integration.

If \( N \) pulses with the same SNR are combined in a lossless coherent integrator, the integrated SNR \( (SNR)_N \) is \( N \) times the single-pulse SNR \( (SNR)_1 \) or

\[
(SNR)_N = N(SNR)_1. \tag{1}
\]

A processing or correlation gain \( G_p \) is defined as

\[
G_p = 10\log_{10} \left( \frac{(SNR)_N}{(SNR)_1} \right) = 10\log_{10}(N). \tag{2}
\]

If the pulse integration is performed during postdetection, where only the pulse envelopes are combined (i.e., magnitude only), then the processing gain is less than the value in (2) and follows a \( \sqrt{N} \) relationship. It is clear that, if a large number of samples are coherently processed, then signals that would otherwise be undetectable without pulse integration can be measured.

Three assumptions are made about the behavior of the amplifier response to allow a pulse integration technique to provide useful results.

1) The device under test (DUT) behavior must be consistent between pulse periods, i.e., each pulse response is identical. If the behavior of the amplifier changes from pulse to pulse, then the technique outlined in this work will provide unreliable results. However, in general, practical devices must meet this requirement, or they would also not be useful in real system designs.

2) The instantaneous bandwidth of the amplifier is sufficient to support fast pulse operation and a phase code signal used to tag the pulses. If an amplifier is considered for use in fast pulse-mode applications, then it must also meet this requirement. The technique proposed is equally applicable to lower speed methods, but such are not demonstrated here.

3) The response of the amplifier is consistent for the different phase states of the phase code modulation used. A phase code is impinged on the pulses applied to the DUT, which allows for correlation processing in the receiver. If the response of the amplifier is different for the various phase states, then the calculated power will be inaccurate.

B. System Block Diagram

The measurement technique demonstrated here involves four primary sections that follow the simplified block diagram shown in Fig. 3. The full details of the system are given in [11]. The first portion is a field-programmable gate array (FPGA) responsible for timing and control. The second section is a transmitter that generates fast pulse-modulated signals with a code impinged on each pulse. The third portion is a receiver that is capable of providing measurement gates with the same
fast transition times as the transmitter. It provides a very high
on/off ratio to allow detection of very small signals, even when
the input signal is very large outside the measurement gate. The
fourth portion is the digital receiver section and the associated
signal-processing algorithms.

C. FPGA Block Diagram

An FPGA is used to provide synchronization between the
timing/control signals and generate the code that is applied to
the transmitted pulses. It is responsible for providing the phase
code, digitizer sample clock, and a trigger signal to synchronize
the timing pulse generators that control the transmit and receive
gates. The timing for the FPGA is controlled by a master clock
signal $CLK$, which is a 24-MHz square wave. The detailed
timing diagram depicting the relationship between the various
signals is shown in Fig. 4.

A maximal-length pseudorandom noise (PN) code is used
as the modulation code in this system and is generated by the
FPGA. A PN code is attractive, because very long code se-
quences can be generated without repetition, which is useful in
gathering long data sequences. Additionally, the autocorrelation
properties of the PN sequence are very good, resulting in low
correlation values for any shift in code.

The PN signal $PSQ$ is generated using a linear feedback shift
register in the FPGA. A shift register with length $N = 28$ and
feedback tap set for a maximal-length code is used. The code
generated has a clock pulse repetition period of
$$M = 2^N - 1 = \frac{268,435,455}{2^6} = 268,435,455.$$ The chip period is 2 $\mu$s, which translates to a
maximum measurement time of $\sim 536$ s before the code is
repeated.

A trigger signal $TRG$ is generated by dividing the master
clock signal by 48 to create a 0.5-MHz square wave. This
signal is required to provide synchronization between the PN
code and the timing signals that control the receiver ($RXQ$) and
transmitter ($TXQ$).

A square-wave digitizer sample clock $SCLK$ is created by di-
viding the master clock signal by two, providing an IF sampling
rate of 12 MHz. The $SCLK$ signal is used to trigger a pulse
generator that outputs a delayed version of the sample clock
$SCLKD$. This additional pulse generator is used to provide fine
resolution positioning of the sample clock to keep the relative
sample position fixed within the receiver gate as it is moved in time. The delay of signals SCLKD and RXQ vary according to the sample point measured in the pulse power profile.

D. RF Block Diagram

The simplified block diagram of the RF section (transmitter and receiver) of the measurement setup is shown in Fig. 5. The components in the transmitter and receiver chain are chosen to operate within the S-band. Bandpass filters are used to provide higher selectivity to the transmitter and receiver sections. The band of operation can then easily be modified by changing the filters and performing a new calibration.

E. Receiver Design

The superheterodyne receiver topology is chosen to provide higher rejection of the switching transients inherent in pulsed systems. The first element in the receiver front end is a high-power RF switch that is capable of dissipating up to 10 W of input power with switching speeds similar to those of other pulse modulators. Two additional pulse modulators (not shown) follow the input high-power switch to provide more than 130 dB of isolation before the first low-noise amplifier (LNA). The LNA in the system has a noise figure of $\sim 1$ dB at 3 GHz. Additional pulse modulators and another amplifier follow the input LNA in the RF front end. The total receiver on/off isolation is greater than 200 dB, which is important for overall system sensitivity. A high-IP3 downconversion mixer is used to convert the carrier from $f_{RF}$ to $f_{IF}$. An IF frequency of 315.5 MHz is chosen due to the availability of IF filters and the ability to reject switching transients through high-pass filtering in the RF front end.

F. Transmitter Design

The transmitter section begins with a frequency synthesizer that generates a CW signal at frequency $f_{RF}$ in the S-band. The measurements shown in this work are performed at $f_{RF} = 3$ GHz. A binary phase-shift keying (BPSK) phase code is applied to the CW carrier. The input signal is amplified and pulse modulated to achieve a high on/off ratio of approximately 120 dB.

The power level at the input to the receiver drastically changes as the position of the receiver gate is moved to overlap with the transmit gate. A 110-dB programmable step attenuator is used to provide full coverage of the attenuation levels required to prevent the receiver from saturating under gate overlap conditions. A static attenuator is used, as necessary, prior to the programmable attenuator to prevent damage to the device.

G. Digital Receiver Design

The signal is digitized using an undersampling receiver topology. The theory of undersampling (which is sometimes referred to as subsampling, bandpass sampling, or direct RF/IF sampling) involves sampling a signal at a rate of at least twice the information bandwidth and using the effect of aliasing to downconvert the signal [12]. The local oscillator (LO) frequency is set to $f_{LO} = 3.3156$ GHz to provide an IF output signal at 315.6 MHz. The effective sampling rate, which consists of the digitizer sample rate and decimation, is 0.5 MHz, which aliases the IF signal to 100 kHz. The 100-kHz offset is chosen to place the aliased signal approximately at the center of the discrete-Fourier-transform bandwidth after digital signal processing.

The analog-to-digital converter (ADC) used in an undersampling system must have an analog bandwidth that is capable of supporting the full IF information band, even if a slow sample rate is utilized. An Acqiris DP240 digitizer card that has a front-end analog bandwidth of 1 GHz and 8 bits of resolution on its two channels is selected. The digitizer also supports a large acquisition memory depth of greater than 8 million points per channel. The large memory depth is important for sampling multiple consecutive pulses to perform the coherent integration required to detect very low level signals.

H. System Construction

The full RF section of the pulse profile measurement system is shown in Fig. 6. Each block of the transmitter and receiver is housed in an individual Faraday shielded enclosure to prevent stray signals from unintentionally leaking around elements.
delay. The appropriate sample number is determined for the varied to measure the power at different points in time, resulting throughout the test sequence. The position of the receiver gate is used for informational purposes only. The other 21 samples are sample is the only valid sample, and the other two samples are and falling edges of the pulse, as shown in Fig. 4. The center for three samples to fit within the output IF pulse. One sample is and edge of the pulse, as shown in Fig. 4. The center for three samples to fit within the output IF pulse. One sample is maintained between blocks to achieve the desired system performance.

III. SIGNAL PROCESSING AND CORRELATION ALGORITHM

The algorithm used to correlate the received signal and calculate the power value is shown in the block diagram shown in Fig. 7. An external clock mode is used for the digitizer since the undersampling technique requires that the sample clock be phase locked to the RF and LO signals, so that the sample is taken in the same location on the IF waveform for each period. A stable 10-MHz reference is shared between the RF, LO, and clock generation sources to maintain the necessary phase lock.

A. Determine Reference Position

The digitized data are analyzed to determine the first transition of the PSQ signal, which is a known location in time with respect to the transmitter pulse. The first transition of the acquired PSQ signal is detected, and the samples are numbered from 1 to 24 from this point forward, as shown in Fig. 8.

B. Decimate Signal

The receiver pulse width is 250 ns, resulting in the possibility for three samples to fit within the output IF pulse. One sample is placed at the center of the output IF pulse through the use of the SCLKD sample clock. The other two samples are on the rising and falling edges of the pulse, as shown in Fig. 4. The center sample is the only valid sample, and the other two samples are used for informational purposes only. The other 21 samples are digitizing noise and do not contain valid information.

The position of the transmitter gate and phase code signal is kept fixed, so that the conditions on the DUT are consistent throughout the test sequence. The position of the receiver gate is varied to measure the power at different points in time, resulting in the valid sample number changing as a function of receiver delay. The appropriate sample number is determined for the receiver delay position, and only this sample of the IF signal and phase code is retained.

The pulse-processing algorithm correlates one sample within each pulse with the phase code value during the pulse. Therefore, the signal must be decimated by a factor of $D = 24$ to retain a single sample. Let the original sampled voltage sequence of the phase code and IF output be $v_{\text{PSQ}}$ and $v_{\text{IF}}$, respectively. Then, the decimated signals are related to the original sequence through the decimation rate $D$ as

$$
\begin{align*}
v_{\text{PSQ},D}[n] &= v_{\text{PSQ}}[nD + i_{\text{ref}}] \\
v_{\text{IF},D}[n] &= v_{\text{IF}}[nD + i_{\text{ref}}]
\end{align*}
$$

where $i_{\text{ref}}$ is the index to the first valid sample within the pulse.

C. Correlate

A BPSK phase code is applied to the transmitted signal, resulting in a signal that is either positive or negative at the receiver. The signal can be demodulated by simply multiplying the received signal by an appropriate delayed version of the normalized phase code values. The phase code values must be normalized (1 or −1) to avoid altering the magnitude of the received signal since the goal is to determine the power of the received signal. The correlator output is

$$v_{\text{corr}}[n] = v_{\text{IF},D}[n]v_{\text{PSQ},D}[n - R], \quad R = 0, 1, 2, \ldots$$

The power calculated from the algorithm in Section III is referenced to the input of the digitizer card and must be calibrated to move the reference plane back to the output of the DUT.

D. Power Spectral Density (PSD)

The PSD of the correlated signal is calculated, providing a means of calculating the power of the correlated signal in the presence of noise. The PSD in this system is calculated using Welch’s method of overlapping periodograms [15]. A sample plot of the PSD for one sample position is shown in Fig. 9.

The PSD covers the frequency range up to $f_s/2 = 250$ kHz. The power of the signal at 100 kHz is found by integrating the PSD over the effective correlation bandwidth, as shown by the shaded area in Fig. 9(b). The signal power calculated is defined at the reference plane at the input to the digitizer card and must be calibrated to move the reference plane back to the output of the DUT.

IV. CALIBRATION

The power calculated from the algorithm in Section III is referenced to the input of the digitizer card. The desired result is the pulse profile at the output of the DUT. Therefore, the power calculated must be compensated for the system gain and loss to move the reference plane back to the output of the amplifier (see Fig. 5). The gain (or loss) after the output of the DUT is divided into four main sections, and the total RF gain of the system is defined as

$$G_{\text{RF}} = G_{\text{StaticAtten}} + G_{\text{ProgAtten}} + G_{\text{RX}} + G_{\text{IFCable}}$$
where $G_{\text{StaticAtten}}$ is the gain of the static attenuator immediately following the DUT, $G_{\text{ProgAtten}}$ is the gain of the programmable attenuator, $G_{\text{Rx}}$ is the conversion gain of the receiver, and $G_{\text{IFCable}}$ is the gain of the coaxial cable connecting the IF output to the digitizer input port. The values for $G_{\text{StaticAtten}}, G_{\text{Rx}},$ and $G_{\text{IFCable}}$ remain fixed for all receiver delay values. The value of $G_{\text{ProgAtten}}$ is varied, depending on the available input power to the receiver to keep the receiver from saturating during full overlap conditions of the receiver and transmitter gates.

The sample clock jitter in the system has the effect of spreading the power of signals in the frequency domain. The total power of the signal is unaffected. Therefore, the peak of the signal is reduced in the PSD when processing a signal with no phase coding. The correlation process serves to despread the signal in the frequency domain. However, the signal peak remains at the same value. The amount by which the signal power is reduced compared to the true value remains constant for any input signal level. Therefore, a static offset value is used to compensate for the jitter loss.

The power measured at the reference plane of the digitizer is referenced to the output of the DUT by subtracting the gain of the RF receiver and the jitter gain. Therefore, the power at the reference plane of the DUT is

$$P_{\text{DUT}} = P_{\text{corr}} - G_{\text{RF}} - G_{\text{jitter}}$$

where $P_{\text{corr}}$ is the calculated correlated power from the algorithm defined in Section III, and the other terms have previously been defined.

The power measurement accuracy and repeatability are influenced by the SNR of the measured signal. The accuracy is better than 0.1 dB, and the repeatability variation is less than 0.4 dB under nominal SNR conditions [11]. An Agilent E4440A spectrum analyzer is used as the reference for power measurements. The measurement sample size is increased in low-SNR regions to maintain these specifications. The linearity of the system is better than 0.1 dB if the signal is kept within the linear regions of the RF receiver and ADC.

V. EXPERIMENTAL RESULTS

A. Microwave Power L0203-41

The final power amplifier in the pulse profile measurement system is a 2–3-GHz 12-W Microwave Power, Inc. (MPI) L0203-41 linear amplifier with an integrated pulse modulator that is capable of generating pulses with typical rise/fall times on the order of 20–30 ns, as specified by the manufacturer. A TTL control pulse with a width of 250 ns and a PRI of 2 $\mu$s (12.5% DF) is applied to the transmitter section to generate an output RF pulsewidth of approximately 240 ns.

The pulse power profile for the MPI amplifier is shown in Fig. 10. The pulse is sampled in 5-ns steps within the pulse time and 10-ns steps elsewhere. The total measurement time is 5.5 h using a 3.0-GHz Pentium-4 computer for 187 time measurement points. A single time point takes approximately 15 s to gather using the minimum number of correlated data points. Additional data samples are taken in the low-power regions to improve the repeatability of the measurement.
The results using the VHSPPM technique illustrate the pulse behavior over a range greater than 160 dB. The minimum sensitivity is approximately $-120$ dBm, even when the peak signal is 42 dBm outside of the measurement gate. The power profile is compared to the traditional measurement techniques using a diode detector or a peak power meter. An Agilent N1912A peak power meter is used as the industry benchmark for comparing this work’s results to peak power meter results.

The accuracy of the technique is demonstrated by comparing the peak power level of the pulse for the three different measurement techniques. The maximum power of the pulse is measured to be 42.5 dBm using the VHSPPM technique, compared with a result of 42.4 and 42.3 dBm for the diode detector and peak power meter, respectively. In particular, the power on the rising and falling edges of the pulse tracks well for the three measurement techniques within their respective dynamic ranges.

The initial turnoff rate of the amplifier is dominated by the pulse modulators in the transmitter. Two different rates of decay appear in the further-out turnoff characteristics of the amplifier. A fast decay rate appears in Region 1, which is defined as the time range from 200 to 260 ns. A slower decay rate is seen in Region 2, which is defined as that from 260 to 550 ns. A linear least-squares curve fit is performed for the two regions and is shown in Fig. 11. The rate of decay in Region 1 is 2.12 dB/ns, compared with the slower decay rate of 0.06 dB/ns observed in Region 2. The determination of the physical phenomenon causing the behavior in these different regions is beyond the scope of this work, although drain lag in the FET is a likely culprit.

Knowledge of the turnoff power characteristics is important to the system designer. Consider an application where the pulse power must dissipate to a level that is 150 dB below the peak level 250 ns after the falling edge of the pulse. In this example, the power difference is 146 dB for the MPI amplifier and does not meet the requirement. The other measurement techniques do not reveal this characteristic.

**B. GaAs pHEMT 50-W Monolithic Microwave Integrated Circuit (MMIC) Amplifier**

A second device is tested to show that the technique is valid for additional devices. The second device is a 2–3-GHz custom GaAs pHEMT MMIC linear amplifier with an integrated drain pulse modulator. The pulse conditions are the same as those in the previous device, yielding an output pulsewidth of approximately 240 ns and a peak power of more than 50 W. The device is driven by an attenuated version of the MPI amplifier output pulse.

The pulse profile for the pHEMT amplifier is shown in Fig. 12. The total measurement time is 2.8 h for 207 time measurement points. The peak power results using a standard peak power meter are also plotted as a comparison showing the accuracy of the measurement within the power meter dynamic range.

The pulse profile for the pHEMT MMIC amplifier shows three distinct regions with different time constants. The initial turnoff is fast in Region 1, which is defined to be from 200 to 250 ns. A slower decay rate is observed in Region 2, which is defined to be from 250 to 350 ns. Finally, a very slow rate is seen in Region 3, which is defined to be from 350 to 1000 ns. A linear least-squares curve fit is applied to the three regions, and the results are shown in Fig. 13. The decay rate in Region 1 is 2.37 dB/ns, which is comparable to the initial rate seen for the MPI amplifier. The decay rate in Region 2 is 0.078 dB/ns. This region is slightly faster than the MPI amplifier, but the actual region definition is much smaller. Finally, a very slow decay rate of 0.026 dB/ns is seen in Region 3.
VI. SUMMARY

A VHSPPM technique has been demonstrated. The measurement technique outlined offers a significant advantage over traditional methods by extending the effective range of the measurement and allowing for short pulsing conditions. The basis for the improvement stems from adding a pulse coding scheme and coherent integration of multiple pulses to allow for an improvement in the measurement SNR. A full description of the system design has been presented with a detailed explanation of the main system elements, including the FPGA, correlation receiver, coding transmitter, and digital receiver.

Measurement results have been presented on typical pulsed power amplifiers to prove the validity of this technique on actual devices under fast-pulsing conditions. The system achieves a full measurement range of greater than 160 dB. The measurement results are compared with the pulse profile results obtained using the standard methods of a diode detector or peak power meter. This technique offers a significant advantage to the system designer, who must characterize the pulse profile of the output power amplifier for use in high-dynamic-range systems since the alternative techniques do not sufficiently reveal the behavior of the amplifier.

ACKNOWLEDGMENT

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U.S. Department of Energy’s National Nuclear Security Administration under Contract DE-AC04-94AL85000.

REFERENCES


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