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# Design of a Low Voltage Appliqué Sensor Interface Module (LV ASIM)

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**Incorporating plug-and-play avionics into a small satellite has many challenges. For smaller classes of satellites, the gains weighed from utilizing plug-and-play (PnP) are overshadowed by the size and power issues associated with supporting PnP. Traditional SPA (Space Plug-and-play Avionics) architectures have utilized separate boards to support the data network, test bypass network, timing distribution, power distribution, and SPA-to-sensor bridges. PnP Innovations has developed an alternate PnP topology which is more suitable for smaller classes of satellites, and still retains the key features of SPA. PnP has developed a low voltage version of the ASIM, the historical sensor-to-SPA bridge. In this newly designed version, the ASIM has incorporated into it a three port SpW router, which eliminates the need for a separate SpaceWire router board. With the elimination of this board, savings in space and power are realized. A similar approach has been incorporated for the timing distribution, and test bypass network. The implementation of these sub-systems have been designed into the ASIM itself, eliminating the need for separate boards to handle distribution of time synchronization signals and test data injection. By utilizing this low power ASIM, Cubesat implementers are now offered a viable option for implementing SPA.**

## I. Introduction

THE traditional needs for space systems have created a breadth of satellite classes. Large geosynchronous communications satellites weighing over 6000 kg (kilogram) and handling tens of kilowatts of power have satisfied US requirements, but at a cost of $300M to over $1B. Smaller tactical and science satellites operating on one to two kilowatts of power have cost between $50M and $300M. This range of satellites have provided the United States with unquestioned space superiority. Indeed, recognition of the excellent cost to value ratio of small tactical satellites has spawned the whole new area of Responsive Space. In addition, new smallsat concepts are gaining acceptance as viable space systems capable of providing useful, cost effective, scientific and military data. These small satellites range from 4 kg cubesats to 50 kg smallsats. This paper focuses on the design of a novel ASIM which can be an enabling component for pushing SPA into cubesat architectures.

## II. Background

Business as usual over the past decades has been to create "hand crafted" satellites, built and tested from the ground-up each time because of risk aversion and a total commitment to unquestioned mission success. A more contemporary model suggests that we should strive to move in the direction of reliable, low-cost solutions that can be assembled rapidly, but also offer high performance (potentially through the ability to acquire support components driven by a more competitive marketplace). That marketplace will emerge if sufficient enterprises open up to foster rapid assembly processes. AFRL, ORS and NASA are leading by example and taking those preliminary steps through initiatives such as the MSV (Modular Space Vehicles) & RRSW (Rapid Response Space Works) programs.

The Air Force Research Laboratory at Kirtland AFB in Albuquerque has led one of the most aggressive efforts to develop standards and technologies to facilitate rapid development, testing and assembly of satellites. This initiative commenced with an objective look at the areas of the spacecraft development process that inhibit rapid deployment of assets. Responsive access to space (e.g. the launch vehicle) is one of the greatest barriers, but the lack of widely accepted standards for hardware and software interfaces is typically the cause of much of the

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customization and associated cost involved in the development of a new mission. Even though the same hardware may be utilized on many generational missions, a particular implementation typically uses a specific collection of hardware - and those hardware elements will be supported by avionics (typically interface cards in a chassis) that require the authoring of specific drivers to facilitate use of that hardware. AFRL sought to focus primarily on the interoperability and tools aspects of the problem when they embarked on the Space Plug & play Avionics (SPA) initiative. SPA defines a common standard for both hardware and software elements of a system. The physical SPA connection to a hardware device in the system consists of a defined data exchange mechanism, supply of power, and the distribution of timing. SPA also defines a common mechanical mounting approach for physical components that facilitates unambiguous assembly of a satellite from PnP parts on a modular structure (a 5x5cm bolt pattern). Incorporating the SPA infrastructure components within these spacecraft structural panels allows much of the labor intensive integration of spacecraft support devices (processors, sensors, actuators, and payloads) to be reduced to a no-nonsense attachment and single pig-tail harness connection to the system.

While CubeSats are among the simplest class of spacecraft, most are painstakingly built using custom devices. The idea of extending SPA concepts to this class of satellites seems very attractive. This would enhance the availability of interchangeable parts and further reduce the cost and time to develop useful systems. In previous SPA instantiations, the ASIM has served as the SPA to component bridge. The ASIM handles the SPA interface protocols, while offering developers enough features to satisfactorily interface with their custom device or sensor. This paper focuses on the development of a Low Voltage ASIM which would be suitable for interfacing to the types of components typically found on a cubesat.

## III. Low Voltage ASIM Design

The design of a Low Voltage ASIM initiated with adapting or modifying the existing Gen2 SPA-S infrastructure hardware (SpaceWire router, Test Bypass Router, and ASIM) to support the lower bus voltage and lower power availability of a CubeSat. Improving SWaP (Size, Weight, and Power) of SPA-S Infrastructure Components to better fit within the CubeSat paradigm has led to several compromises. For the Test ByPass and SpaceWire routers, these functions have been incorporated into the ASIM itself, thus eliminating the need for a separate stand-alone SpaceWire router or stand-alone Test ByPass router. In order to utilize these functions on the ASIM, dual SPA connectors are required.

Shown in Figure 1 is an example implementation for how we envision the ASIMs to be interconnected. By utilizing the dual SPA links, the ASIMs can be daisy-chained together. This daisy-chaining provides the necessary linkage of SpaceWire data and Test ByPass data. Thus, by incorporating the necessary functions onto the ASIM itself, the requirements for a separate SpaceWire router and Test ByPass router board have been eliminated. If a connection to a Test Computer is not required or not warranted (as in the actual flight configuration), it can simply be removed. The daisy-chained components can be closed to form a full ring connection.

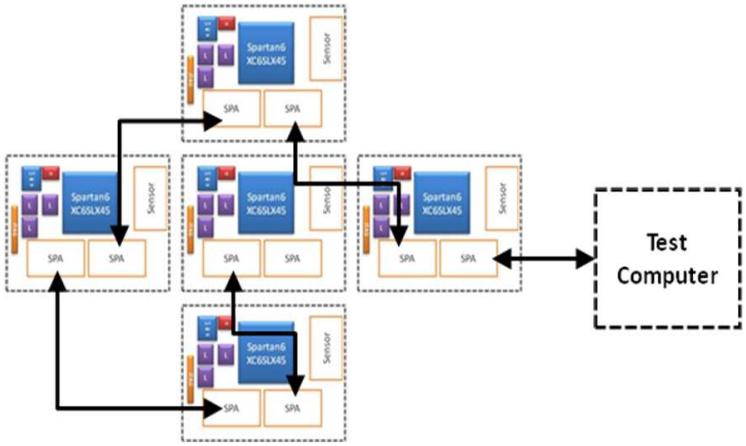


**Figure 1. Example Implementation Using Dual SPA Connectors**

If a more traditional implementation is desired, the LV ASIM can be connected to employ only one of the SPA connections. This type of connection will require a SpaceWire router to be present, but could be preferred in various implementations. Furthermore, if a separate SpaceWire router is utilized and higher data throughputs are desired, then both SPA connections (the SpaceWire portion) can be connected to the same SpaceWire router. The LV ASIM can be configured to use whichever SpaceWire link has available bandwidth. This type of arrangement would only be used in high bandwidth applications, such as a camera or other payload interface. Each of the SpaceWire links on the LV ASIM can support link speeds of 200 Mbps. By coupling both of these together, the LV ASIM can support a 400 Mbps data connection.

## IV. Low Voltage ASIM Features

Shown in **Error! Reference source not found.** is a block diagram for the LV ASIM. For clarity, not all of the interconnections between the Spartan 6 FPGA and the external chips are shown. However, as the Spartan 6 forms the heart of the LV ASIM, most devices have an implicit connection with the FPGA.

The features of the LV ASIM will be discussed in the following sections.

### A. Spartan 6 FPGA

The LX45 Spartan 6 FPGA was selected as a good tradeoff between performance and power. The Spartan 6 is manufactured on a 45 nm, 9 metal layer process. The LX45 contains approximately 55,000 flip flops and 116 internal blocks of 18 kb memory. The size of the FPGA can easily accommodate an embedded 32 bit microprocessor, as well as provide ample RAM for execution.

Contained within the Spartan 6 is the MicroBlaze soft-core processor. This 32 bit embedded processor is capable of performing up to 100 MIPs. This will offer a magnitude improvement over existing 8 bit based ASIMs, while maintaining a low power consumption profile. The required peripherals for the MicroBlaze have been converted into the bus interface necessary to interface directly with the processor. This work was done at the interface layer; redesigning the innards of the peripheral was not required.

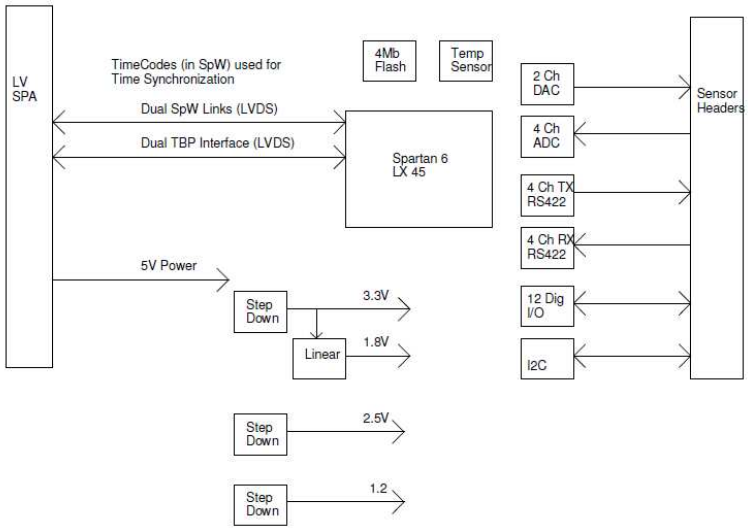


**Figure 2. LV ASIM Block Diagram**

The low-voltage ASIM will be required to support a larger portion of the computing load, and as such, a more powerful softcore processor (MicroBlaze) was integrated into the ASIM. The MicroBlaze represents a move from an 8 bit based processor on the Gen2 ASIMs (8051 legacy) to a modern 32-bit RISC based processor.

### B. Power Distribution Network

The LV ASIM accepts nominal power input of 5 volts ± 0.5 volts. The input voltage is stepped down to 3.3, 2.5 and 1.2 volts via a Linear Tech LTC3406B synchronous buck step down regulator. The regulator has a very high efficiency (up to 96%), and is able to supply 600mA of current at each voltage.

The 1.8 voltage network is derived from a linear voltage regulator. The amount of current required for the 1.8 voltage network is small, and is only used for brief amount of time while the FPGA is being configured from the configuration EEPROM.

### C. RS422

Four RS422 transceiver chips are incorporated into the design. Support for the RS422 protocol was incorporated into the design because it is a common protocol typically utilized for communications. Each RS422 chip contains a full duplex communication channel. The channel can be placed into a power savings mode when not utilized. The RS422 transceiver chips are rated for up to 20 Mbps, and only draw 5 µA when in power savings mode.

### D. Flash Memory

A Winbond Electronics 4Mb (512 kB) serial flash chip is included on the board. This flash chip will serve to contain the xTEDS and program code. Upon boot-up, a bootloader module transfers the contents of program code from the external flash memory chip to the local internal BRAM. This is done for speed and power savings considerations. Additionally, by hosting the program code in external flash memory, the ability to upgrade the

program code *in situ* is realized. The flash memory is allocated for 256 kB of program code storage, 128 kB of xTEDS storage, and 128 kB of user accessible non-volatile storage. In its power-down mode, this device draws 1 µA.

### E. Temperature Sensor

A National Semiconductor LM70 type digital temperature sensor is included with the LV ASIM. A temperature sensor can provide important data if an area of the satellite is operating outside the temperature envelope. This temperature sensor provides accuracy of ± 0.25 ºC. This temperature sensor can be placed into a low power consumption mode when not utilized. In such mode, the device will consume less than 10 µA.

### F. Mixed Signal Support

The LV ASIM supports four ADC channels and two DAC channels. The ADC channels have an input range of 0 to 3.3 volts, while the buffered DAC channels can drive over a 0 to 5 volt range. Both devices are communicated with using separate serial buses. The ADC provides 12 bit resolution while the DAC utilizes 10 bit resolution. Both have a power-down state when not utilizing these features.

### G. Digital I/O

The LV ASIM includes twelve digital I/O lines which may be configured for a variety of purposes, including serial ports, $I^2C$, synchronous serial, etc. The digital I/O lines are protected by a series 20 Ω resistor.

### H. Integrated Power Switch

The LV ASIM includes an integrated Load Switch for controlling power to the device. The switch turns on or off the +5V main power to the device. The $R_{dson}$ (the drain-source on resistance for the FET) is typically 55 mΩ, and can handle 2.8A of current.

### I. Serial Debug Interface

The LV ASIM includes a dedicated serial port debug interface. This interface is useful for console style terminal output. The gen2 ASIM makes heavy use of the debug console for development and debug. A separate Molex style 3 pin connector is used to easily connect to a standard PC serial port. The LV ASIM includes the necessary circuitry to directly drive the PC serial port and requires no special adaptor.

## V. LV ASIM Interfaces

There are several key interfaces for the LVASIM. The SPA side interface includes the two SPA connectors, and the User Side interface includes connector interfaces for communicating with devices.

### A. CubeSat SPA Interface

Shown in Table 1 is the pinout utilized for each of the dual SPA connectors. The connectors chosen are vertical mount Series 89 Nanominiature connectors from Glenair. The LV ASIM utilizes the socket connector, part # 890-007-15S.

Note that only three of the four typical subsystems in SPA are shown. The SPA subsystems usually include Power, SpaceWire, TBP (Test ByPass) and PPS (Pulse Per Second) or Time Synchronization. Absent from the LV SPA-S pinout is time synchronization. In order to conserve signal pinouts and board space, this was intentionally omitted from our implementation of SPA-S. However, this does not mean that SPA-S must forego a proper time synchronization subsystem. Rather, the time synchronization is handled by the SpaceWire signaling. Built into the original SpaceWire standard itself is a mechanism to distribute one byte of high priority data to all points on a SpaceWire network. This distribution of a byte of data serves the same function as the rising edge in a discrete (RS422) implementation of a time synchronization system. Thus, the LV SPA-S implementation preserves the spirit of SPA by handling all the subsystems. The primary penalty of utilizing this mechanism for time distribution is an additional latency. Thus, the measured difference for 'time' is approximately 1.3 microseconds for each additional router hop the LV ASIM encounters. However, as this is a deterministic parameter, the value can be zeroed out, by adjusting the contents of the time synchronization SpaceWire message to reflect the known delay.

**Table 1. SPA-S CubeSat Pinout**

| Pin # | SubSystem | Signal Name |
|---|---|---|
| 1 | SpaceWire | DataIn+ |
| 2 | SpaceWire | StrobeIn+ |
| 3 | SpaceWire | DataOut+ |
| 4 | SpaceWire | StrobeOut+ |
| 5 | Power | +5V |
| 6 | TBP | FromHost+ |
| 7 | TBP | ToHost+ |
| 8 | TBP | TBPEnable |
| 9 | SpaceWire | DataIn- |
| 10 | SpaceWire | StrobeIn- |
| 11 | SpaceWire | DataOut- |
| 12 | SpaceWire | StrobeOut- |
| 13 | SpaceWire | GND |
| 14 | TBP | FromHost- |
| 15 | TBP | ToHost- |

### B. User Interfaces

The User Interfaces are encompassed into three header interface connector: J5, J6, & J7. J5 provides Digital I/O access, J6 provides RS422 access, and J7 provides mixed signal support.

The User Interface connection points are based on 0.050" dual row pads. Optionally, a Samtech style connector can be assembled onto any of the connection points.

## VI. Test Results

The LV ASIM was built and tested with a basic set of peripherals. Shown in Figure 3 is the fully functional prototype board. Seven initial prototypes were built. The prototypes were configured with the MicroBlaze embedded processor and a basic set of peripherals. An expansion board is currently being built, which will provide the LV ASIM with a CameraLink interface, SVGA Display Driver, and additional on-board external SRAM.


**Figure 3. LV ASIM Prototype Board**

The base system clock for the LV ASIM is a 50 MHz oscillator. Currently, the MicroBlaze utilizes this clock as the main system clock. Because the *dynamic* power draw is a directly related to the clock frequency, using a 10 MHz clock would reduce the *dynamic* power consumption to approximately 1/5th of the existing values. Current measurements were performed when the LV SPA board was placed into different configuration scenarios. These results are shown in Table 2.

**Table 2. LV ASIM Total Power Consumption**

| LV ASIM Scenario | Supply Voltage [V] | Supply Current [mA] | Power [mW] |
|---|---|---|---|
| FPGA Unconfigured | +5V | 18.7 | 94 |
| FPGA Configured with single light blinker | +5V | 19.1 | 96 |
| FPGA Configured with RS232 loopback | +5V | 20.2 | 101 |
| MicroBlaze @ 50 MHz, processor halted | +5V | 67.4 | 337 |
| MicroBlaze @ 50 MHz, processor idling | +5V | 71.1 | 356 |
| MicroBlaze @ 50 MHz, processor calculating primes | +5V | 77.4 | 387 |

One of the advantages of our approach is that Flight Software modules developed for other programs can be used in the SPA-S Cubesat Bus with little change. PnP Innovations has developed a laboratory computing system that allows rapid software development. This capability is present at AFRL in multiple testbed areas. The hardware developed in this project was integrated with our integrated computing testbench, as shown in Figure 4, to provide the capability to develop mission application software, test it in a "Flight Software In the Loop" (FSWIL) mode against pure software models of the SPA hardware devices (all on a Windows-based PC). Upon satisfactory results (verification of functional correctness and data interface dependency checking), testing can transition immediately to a very flight-like configuration in which Test Bypassed endpoint simulators represent hardware and the software modules run on SPA computing Nodes. This is "Hardware In the Loop" (HWIL) mode, which may be used to fully assess proper system operation considering the timing and latency peculiarities associated with the flight-like data network and processors.

The physical elements of the SPA-S Cubesat Computing Testbench consist of a PCIe SPA-S host interface card, LV ASIMs, and a SpaceWire & TBP Router. PC host workstations present the tools that allow application developers to author, debug, test, and characterize the performance of PnP software modules. Multiple low-voltage SpaceWire routers can be ganged together just like SPA-S routers to accommodate greater numbers of attached devices or processors.

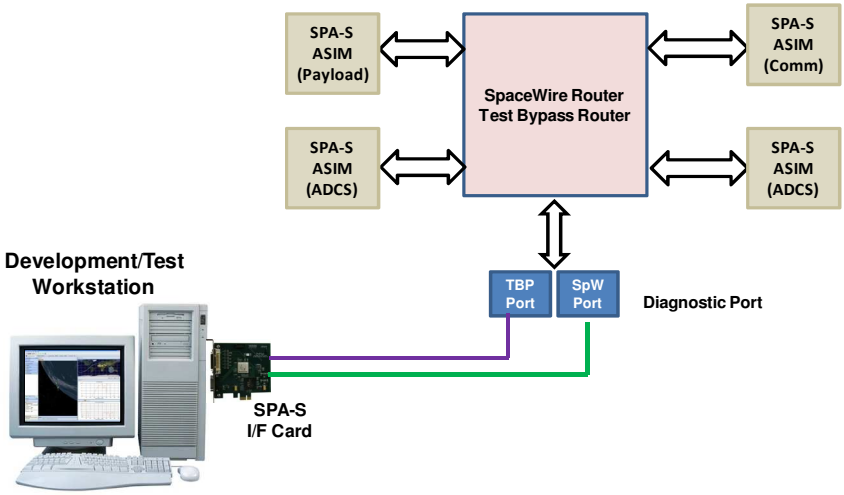


**Figure 4. SPA-S CubeSat Integrated Software Testbench**

The PCIe SPA-S Interface Card allows a host PC to become an endpoint in a SPA system. It facilitates a data connection to the SpaceWire data network with a 300 Mbps link. The card can also be configured to provide the SPA standard time pulse to all endpoints in the system. It also exposes RS-422 ports that support the TestByPass portion of the SPA standard. These ports may be used to supply ASIM-hosted devices with simulated data to support HWIL testing.

Tools resident on Windows-based host PC workstations provide the ability to take SPA application code modules from the prototype phase to flight testing. An essential support element to foster this process is Star Technology Corporation's Spacecraft Design Tool (SDT), which may be easily configured with virtualized models of spacecraft support devices representing a candidate spacecraft. Once these models are loaded, they can be exposed to software in one of two ways. In FSWIL mode, they present as SPA components to the core data system, but originate at a single SpaceWire endpoint (the one attached to the development PC via a SPA-S PCIe Card). In HWIL mode, those same models utilize the TestBypass function of the PCIe Card to deliver simulated data to physical ASIMs so that the ASIMs present SPA interface data consistent with coordinated six-degree-of-freedom simulation orchestrated by the SDT framework. In fact, physical hardware need not even be attached to the ASIMs

to conduct HWIL testing; they may merely serve as "Endpoint Simulators" that serve as placeholders for actual hardware so that software can be comprehensively tested. In this way, full Day-In-The-Life (DITL) studies may be conducted.

SDT also provides a "Data Browser" capability that capitalizes on the xTEDS of the SPA standard to provide a dynamic view into the data system. The Browser is a powerful test support tool, allowing SPA interfaces to be exercised without any configuration – all input and output data points are described by the xTEDS, so command interfaces can be automatically generated and component output data may be subscribed-to and easily manipulated for analysis in GUIs such as numeric displays and strip charts. The Browser is moving toward full ground station capability. Star Technologies and PnP Innovations are working together to realize that ultimate goal.

## VII. Conclusion

The inclusion of a powerful embedded 32-bit microprocessor into the LV ASIM brings an order of magnitude increase in compute power when compared to the Gen2 ASIMs. By incorporating a miniature SpaceWire router and Test ByPass router into each of the LV ASIMs, the need for an external stand-alone routers is eliminated. This elimination can save area, which is an important design constraint in CubeSat missions. Furthermore, the usage of low power components on the LV ASIM offers all of these features at power consumption levels of approximately half that of the Gen2 ASIM.

The design of the LV ASIM fully supports a SPA-S implementation. The +5V Power bus is more suitable for CubeSat missions. The dual SpW links provide ample data connectivity. The Test ByPass support allows for system testing, and the inherent time code support in SpaceWire provides the necessary time synchronization. We are very encouraged by these results and believe they form a strong foundation to build, test, launch, and operate a 3U SPA-S CubeSat.

## Acknowledgments

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