Adaptive Circuit Implementation in FPGAs

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The larger variations in nanometer CMOS technology process is making the concept of designing VLSI circuits at the worst case scenarios less efficient. It results in a design with large power consumption. This concern is more pronounced in FPGAs since a large number of transistors must be used to implement a Configurable Logic Block (CLB) to perform a single logical function. Our proposed technique takes the basic power calculation into consideration, $P=\frac{1}{2}C_L V_{DD}^2 f\alpha + V_{DD} I_{leak}$, and takes advantage of the heavy dependence of dynamic power consumption on supply voltage. By reducing the supply voltage to a point just before the occurrence of erroneous data, one could save power consumption of the circuit substantially. This new design approach improves the performance/power of the FPGA designs.

Our circuit solution is conceptually similar to a Razor circuit solution [1]. This Razor technique is preliminary developed for ASIC type designs, where every time an error occurs, the clock is stalled for one cycle and the entire computation is repeated. We utilize the same concept of Razor, but improve it to make it possible to implement it in future FPGA fabrics. It can therefore be easily implemented into an FPGA fabric. Figure 1 shows our modified error detection/correction circuit with inherent PVT (Process, Voltage and Temperature) variation protection, where the output will always be the corrected logic even if an error occurs. This approach eliminates the need to stop the system clock for re-computation. This avoids the large amount of logic required in the clock circuitry to incorporate this need based stalling. It is a significant design advantage since clock circuitry itself has very critical design constraints.

Along with this modified error correction technique, a unique adaptive (very low power) solution as shown in Figure 2 has been proposed for non-critical timing applications. This adaptive technique has the ability to step up/down the frequency on an as needed basis. This is highly beneficial for all applications which have non-uniform processing load. By this technique, the system can be switched back and forth from high power-more throughput mode to low power-less throughput mode, on demand. The high power savings that can be obtained through this technique can be explained from the stronger dependence of power over voltage than frequency over voltage.

Reference: [1] T. Austin, D. Blaauw, T. Mudge, and K. Flautner, "Making typical silicon matter with Razor", IEEE Computer Magazine, March 2004.

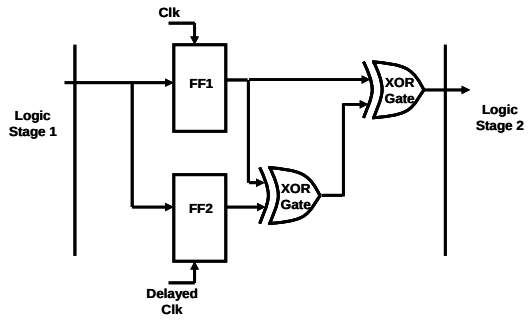

Figure 1: Proposed Error Correction Design

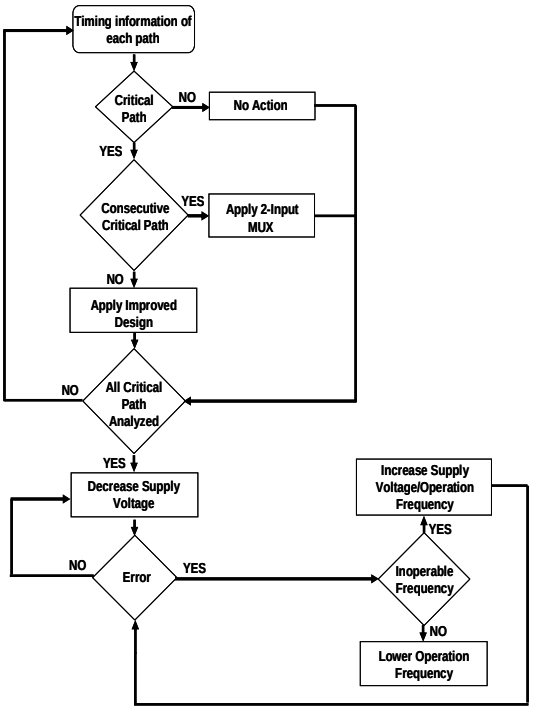

Figure 2: Adaptive System Algorithm