DESIGNER'S INTERFACE

EDUCATIONAL USES OF FPGAs

Since 2000, the Department of Electrical and Computer Engineering at The University of New Mexico (UNM) has been using field programmable gate arrays (FPGAs) and programmable logic tools in many of its computer engineering undergraduate and graduate courses. The Xilinx University Program (XUP) supported a large portion of UNM's efforts.

In the fall of 2000, students in the introductory digital logic course began using Foundation 2.1 software on XC4000 FPGA and XC9500 CPLD devices. Since then, UNM has taught VHDL, FPGA, and CPLD technology in follow-on undergraduate courses in digital design, VHDL programming and senior design and graduate courses in VLSI and computer architecture. Students are currently taught digital logic using ISE 5.2 to develop projects for the Spartan2E FPGA and CoolRunner CPLD devices. UNM has developed online tutorials for a number of advanced reconfigurable logic tools such as Coregen (prepackaged VHDL modules), XPower (power consumption estimator), and Floorplanner (tool for CLB/IOB analysis).

More recently, with the support of the XUP, UNM has developed online tutorials for teaching digital system design using the System Generator (Sysgen) and the Embedded Development Kit (EDK). Sysgen is a supplement to MATLAB's Simulink, which allows graphical development of DSP projects that it then transfers to programmable logic. EDK allows users to develop projects involving virtual Microblaze microprocessors into FPGAs and the programming of PowerPC microprocessors into Virtex2 Pro FPGAs.

Donald W. Bouldin, Editor

In conjunction with the XUP, UNM has designed an eight-layer dual Virtex FPGA prototyping platform. The board is currently being tested at the U.S. Military Academy (West Point), the University of Texas (El Paso), and the University of Texas (Austin). This board is designed to fill the need for versatile programmable platforms at a more advanced level without being excessively expensive.

UNM is constantly assisting the XUP to promote advanced studies and the ability to develop new teaching methodologies at other universities. Annual professors workshops at UNM allow academic instructors the ability to exchange teaching taxonomies, see what UNM can offer, and obtain briefings on new state-of-the-art hardware and software (free of charge). UNM representatives will also travel to assist in these areas. As part of their ongoing efforts to assist other universities in developing their own programmable logic laboratories, UNM recently provided presentations at the Pan-American Studies Institute in Bolivia. All developed tutorials, associated source code, and other information are available (free) for any educational institution.

The driving personnel at UNM for all these efforts are: Dr. Marios Pattichis, Dr. Howard Pollard, Jorge Parra, Alonzo Vera (alonzo@eece.unm.edu), and Craig Kief (kiefc@eece.unm.edu). The following Web site provides a central location for obtaining all desired information:

http://www.eece.unm.edu/xup/xup_unm_links.htm

SCHEMATIC-DRIVEN INTEGRATED CIRCUIT DESIGN TOOLS

The popular MicroMagic toolset has now been placed in the public domain such that anyone (universities and companies) can download them at no charge under a BSD license.

Schematic User Environment (SUE) is a graphical environment that allows users to enter, visualize, and control large, complex chip designs. SUE is the first tool to combine HDL-based functional designs with structural design. SUE understands everything from Verilog down to the operation and physical placement of transistors and wires.

MAX is an extremely fast, industrial-strength, full-custom layout editor with the added benefit of a complete Tcl/Tk interface and API. MAX comes with continuous DRC, connectivity tracing, schematic cross-probing, wiring tool, extraction, schematic-driven layout, and more. MAX reads and writes GDSII.

DataPath Compiler (DPC) allows the user to generate data paths from a schematic view, and back annotate accurate timing information onto the schematic in seconds. DPC can place custom-style "bit slice" data paths minimizing wire lengths for high performance, and can even include control logic, all using your existing standard cell library.

MAX-LS seamlessly integrates the schematic capture of SUE with the MAX layout editor schematic-driven physical layout. It includes interactive cell generation based on LVS and DRC correct layout and can handle the largest SoC IC design databases. Its GDSII output can go directly to mask composition products for IC fabrication.

The Mega Cell Compiler (MCC) allows users to easily build their own generators for SRAMs, DRAMs, ROMs, pad rings, or any other regular or semiregular structure, in just minutes. Verilog, HSPICE, critical path netlists, and timing models can all be generated automatically.

The tools described above run under either the LINUX or SOLARIS operating systems.

For additional information, access:

http://www.micromagic.com

C-TO-FPGA SOFTWARE HALF PRICE FOR UNIVERSITIES

Impulse Accelerated Technologies, Inc. announced university discounts on its CoDeveloper C-to-RTL development tools. CoDeveloper allows embedded application developers to create mixed hardware/software applications using ANSI-C, to partition applications between multiple FPGAs and embedded processors, identify and resolve data blockages, unroll and pipeline C code for parallelism and output synthesizable HDL code compatible with Xilinx, Altera and third-party synthesis tools. CoDeveloper can also generate hardware/software interfaces for Altera Nios, Xilinx MicroBlaze and Xilinx Virtex II Pro (PowerPC). Educational pricing also applies to Impulse CoValidator, a VHDL simulation and coverage analysis tool. CoDeveloper educational prices range from US$2,500 to 5,000. Lower, annual license pricing is also available.

For more information, access:
http://www.ImpulseC.com

OPEN CORE PROTOCOL INTERNATIONAL PARTNERSHIP

Open Core Protocol International Partnership (OCP-IP) provides a common standard for intellectual property core interfaces, or sockets, that facilitates "plug and play" system-on-chip (SoC) design. OCP-IP is an Adoption Group of the VSI Alliance (http://www.vsia.org). A bibliography of major papers and sources in the SoC space is posted on its Web site. OCP-IP has also established a university program in which members receive free access to the members-only portion of the Web site, free software tools, free technical support, and training that is packaged and ready for incorporation into a course or immediate independent use by students. Present members of the program include: Tampere University of Technology (Finland), University of British Columbia, Royal Institute of Technology (Sweden), UC Berkeley, NTHU (Taiwan), STARC (Japan), ECSI, CNFM (France), and others.

For additional information, access:
http://www.ocpip.org

STRUCTURED ASIC PLATFORMS

Structured ASIC platforms are prefabricated ICs except for a few customizable layers. The official definition according to the Structured ASIC Association (http://www.structuredasic.com) is

> an integrated circuit architecture and methodology that delivers reduced entry cost and faster time to silicon using a predefined arrangement of late-stage mask-customizable logic and prediffused macros and IP.

The rapidly increasing costs for masks and the challenges of very deep submicron manufacturing make the initial venture into cell-based ASICs more expensive and riskier than in the past. Whenever performance higher than that provided by field-programmable products is needed, structured ASICs may be the solution of choice. This middle ground that used to served by gate arrays is now re-emerging as platforms with lower cost, shorter turnaround times, and design flexibility or programmability.

The design flow begins with the designer using logic synthesis and simulation to produce a register transfer level net-list based on the available blocks in a predefined platform. The platform vendor then performs the physical placement (actually assignment) and routing tasks, pulls prefabricated wafers from inventory and customizes the upper metal layers using masks or ebeam patterning. This approach isolates designers from many of the physical design issues such as 3-D parasitic extraction, signal integrity, crosstalk, antenna rules, electro-migration, and IR drops.

Vendors offering a variety of these platforms include:

- Altera
  http://www.altera.com
- AMI Semiconductor
  http://www.amis.com
- ChipX
  http://www.chipx.com
- eASIC
  http://www.easic.com
- Faraday Technology
  http://www.faraday-usa.com
- Fujitsu Microelectronics America
  http://www.fma.fujitsu.com
- Leopard Logic
  http://www.leopardlogic.com
- Lightspeed
  http://www.lightspeed.com
- LSI Logic
  http://www.lsilogic.com
- NEC Electronics America
  http://www.necel.com
- ViASIC
  http://www.viasic.com.

Tool vendors supporting this flow include:

- Accelchip
  http://www.accelchip.com
- Magma
  http://www.magma-da.com
- Synopsys
  http://www.synopsys.com
- Synplicity
  http://www.synplicity.com.

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Share your thoughts about this magazine.

Send an e-mail to the Editor-in-Chief.

Letters may be published in future issues and edited for style.