EETimes Market Intelligence Unit

2008 FPGA/Analog Market Survey

INTRODUCTION

Two years ago, Piper Jaffray teamed up with *EE Times* in a survey of FPGA designers to determine trends in semicustom design and device usage. This year, the survey expanded significantly in two dimensions. Piper Jaffray asked new questions of the FPGA designer base on its use of discrete analog components as part of overall FPGA-based systems. The FPGA Mission Assurance Center at Air Force Research Laboratories joined us in asking several questions to a select audience of FPGA designers working on military and aerospace designs.

The survey was conducted by Wilson Research, using a database of *EE Times* readers and Wilson's own ExecStats web-based analytical tools. The survey was conducted in from Aug. 14 to Sept. 10, 2008, with results compiled in September and October. There were 449 general respondents, and 132 specific to military-aerospace. This gives the survey a 95% plus or minus 5% confidence level.

The general survey asked about technology trends in semicustom design at large, including how FPGAs were used as adjuncts or replacements for gate arrays, CPLDs, and cell-based ASICs. We also asked about the underlying technologies used in FPGA programming elements, as well as the soft and hard cores used in the design of devices. Finally, we asked questions specific to vendors within the FPGA community.

The analog portion of the survey sought to define trends in analog component use, and to find out which vendors were meeting varied needs of the design community.

Mil-aero users were asked most of the same questions as the general community. For these questions, we have charted the responses of the specific mil-aero environment immediately following each commercial FPGA user chart. This way, comparisons can be made of the way needs differ in these two communities. A separate series of questions, asked only of mil-aero designers, generated responses that are appended to the end of this study. They dealt with such topics as single-event upsets, the availability of universal scrubbers to correct configuration faults, and the viability of certification programs for users. AFRL's FMAC will use

the information gathered to define its programs for aiding the mil-aero FPGA design community.

RESPONDENT CHARACTERISTICS

The largest group of respondents characterized their organization as "engineering/science/research," a category which obviously can include corporate industrial operations. Aerospace constituted the next highest segment, followed by computer OEM, manufacturing, government/military, communications carrier, and health care. (For military-specific responders, the answers were skewed to aerospace and military.) The size of the respondents' companies ranged widely, from the largest sector (25.6%) in companies under 100 employees, while the second-largest sector (22.2%) represented companies of 20,000 or more employees. Between those two extremes, respondents represented all scaled sizes. Even among general respondents, the industrial vertical sector with the largest percentage of designers was aerospace, followed by datacom/networking, electronic instruments, computers and peripherals, and industrial control.

Job functions among respondents vary widely, and include many different categories (respondents could choose more than one). Hardware and software integration led the pack with 59.0% claiming such duties, followed by debugging hardware (57.6%), architecture selection and specification (54%), designing hardware for embedded systems (52.2%), and prototype testing (52.2%). Chip-level duties such as SoC design ranked significantly lower on this list. In both general and military categories, engineers who described themselves as "hardware engineers" constituted more than half of respondents.

Since the reader lists were selected for FPGA experience, it is no surprise that more than three-quarters of respondents said they worked with FPGAs and analog components. What is more surprising is that only one-third worked with ASICs.

FPGA DESIGN TEAMS AND RECRUITMENT

We asked about trends and recruitment and talent, and immediately discovered that a total of 72.1% of respondents reported some difficulty, great difficulty, or insurmountable difficulty in recruiting adequate FPGA talent. The largest sector, 50.1 %, reported at least some difficulty. General advertising remains the most popular way to find engineers (53.3%), followed by recruitment from other firms, and from graduate or undergrad university programs.

New employees typically take less than a year to get up to speed. Equal numbers (36.3%) reported new employees taking less than six months to learn methods, and six months to a

year. Assembling a project team does not seem to be a time-consuming process, with roughly a quarter (20% in mil-aero) saying a team could be created immediately, and more than 30 percent reporting team assembly takes less than a month. Slightly more than half of respondents in both commercial and military said their organizations would *not* be hiring new engineers in the next year, no doubt a partial response to economic uncertainty. At the same time, close to half of respondents said their managers had no engineering experience in FPGA design.

On-time delivery of product prototypes may not be great, but results are better than those shown in *2008 Embedded* and other recent studies. Respondents claimed that more than 50 percent of projects were on time, with 11.6% commercial and 14.2% military claiming that 100% of their designs had been completed on time. When projects are delayed, however, effects are significant, with more than 70% claiming program delays resulted. What is to blame for these delays? Overall project complexity was cited by more than 55% of both types of respondents, with the lack of skilled engineers coming in a distant second at around 26%.

FPGA CHARACTERISTICS AND PREFERENCES

The first myth dispelled was the so-called "need for speed." More than 85% in both commercial and military realms said speed was not an issue in their designs. For those who thought FPGAs were too slow, most said a 50% speedup would be useful.

Several factors were listed as important for completing designs on time, though none exceeded 45%. The most important was "completing functional verification" at 40.3%, followed by "meeting timing constraints" at 30.6%, and "managing complexity" at 30.3%. The issue of controlling costs ranked only fourth in the list. Few find trouble gaining prototyping platforms, with two-thirds saying this was not an issue.

VHDL remains the primary design language, constituting 43.8% of commercial users and 50% of military users. Verilog is preferred by 29.4% of commercial users, 21.8% of military users. All other methods, including legacy Verilog, MatLab, C, LabView, etc., constituted single-digit percentages in the survey.

Close to 75% of respondents use embedded processors in their designs. More than 70% of these users rely on C/C++ EDK for the processors, followed by embedded Linux and Linux.

In choosing FPGAs over ASICs, users cited two reasons with equal fervor, around the 53% level: time to market and ASIC NRE costs. Production volumes and cost of design tools also rank as important, albeit at significantly lower rates.

Those designers using Xilinx or Altera design tools expressed a desire for tutorials, dominated by teaching on floorplanning. Other popular tutorial topics would be memory management, soft embedded processors, partial reconfiguration, and power management.

Simulation software is utterly dominated by ModelSim, with the SE version being most popular, followed by XE and PE. NCSim is only cited by about 10% of respondents.

We tracked satisfaction levels across several tasks in the EDA domain. In many, a plurality of users were satisfied, but only by thin margins. Rarely did satisfaction levels exceed 50%, usually in well-defined realms such as layout extracting, simulation, and routing. In timing estimation and analysis, 51% of users were dissatisfied, though this number was only 39% among mil-aero users. Testability scored poorly among both groups of users. Power estimation analysis and signal integrity analysis also could use some improvement.

In the field of verification, a definition of terms is important. Users are generally satisfied with physical verification tools, but want to see better hardware-assisted verification, and functional verification tools.

FPGA VENDORS

Many of our questions dealt with FPGA vendors, but discussed vendor technologies and overall trends before moving to specific companies offering FPGAs. Across all vendors, users say they are most satisfied with technology, some 93.5% saying they have a favorable opinion. Generally high marks also were given for ease of use, sales reps, and support. The highest unfavorable ranking was given to licensing (50.7%), followed by pricing, interoperability, and quality of software. It may be comforting to note that favorable rankings exceeded the 80 and 90 percentile, while unfavorable ranking only were mentioned by more than half of respondents on one occasion (for mil-aero users, this was pricing at 57.3% rather than licensing).

There's no denying power consumption is a bigger issue than in the past, with 55% (56% military) saying the issue is more important than a year previous. In this field, Xilinx holds only a slight lead as best vendor, with 27% (33% military), followed by Altera and Actel, both at 22% (in military realms, Actel beats Altera, 25% to 20%).

Xilinx ranks first in high-quality production process node, cited by 43% commercial, 44% military. Altera ranks second, at 27 and 28%, respectively, followed by Actel and Lattice. It is interesting to note Actel's first-place standing in handling radiation-induced upsets – it is mentioned first in commercial designers at 18%, and among military designers at 39%. This is

still a niche area, not used by 60% of commercial and 31% of military designers, but it is an important niche for Actel.

In IP cores, Xilinx holds a significant lead, 54% in commercial and 58% military, with Altera following in the low 20's and all other vendors in single-digit places.

We asked designers what their trend in using semicustom devices would be. In the bar charts, you can visibly observe the mean slip down into decreasing-usage territory as we go from cell-based ASICs to CPLDs to gate arrays. No NRE-based ASIC technology is on the verge of obsolescence yet, but gate arrays in particular have hit a plateau – 65% of respondents said their use would stay the same, 7.2% would decrease somewhat, and 12.8% said gate array use would decrease greatly. Since FPGAs typically are run on more advanced process nodes than ASICs, Piper Jaffray predicts the trends we saw will accelerate in coming quarters.

More than 72% said that FPGAs would increase greatly or somewhat, while 27% said they would stay the same. Almost no one saw FPGAs decrease. Structured ASICs were dominated more than 60% by those that thought their use would stay the same. The prospects for CPLDs were slightly better – just over half thought they would stay the same, and one-fourth thought they would increase slightly. Cell-based ASICs were more lopsided, with 68% (72% in military) thinking their use would stay the same.

For the underlying programming element of the FPGA, the big news is the phasing out of antifuse, and the growing use of flash and SRAM cells. Flash-SRAM hybrids appear to remain a niche. Some 63% of commercial and 51% of military designers say they use no antifuse FPGAs whatsoever. Numbers of those not using flash-SRAM hybrids are almost as high, though those that use them employ them in more designs than antifuse FPGAs. By contrast, 70% of commercial and 72% of military designers use some flash-based FPGAs, with numbers skewed toward percentages of designs in the 20 to 75% range. For SRAM-based elements, larger numbers (36.3% commercial, 28.7% military), report relying on SRAM programming elements for *all* of their FPGA designs.

Satisfaction levels for flash-based devices are impressive – 45.2% expect their use to stay the same, 39.6% to increase somewhat, and 10.7% to increase greatly. Note that this is better than SRAM-based devices, where 49% see them staying the same, 30% increasing somewhat, and 8% increasing greatly, leaving 13.1% anticipating some level of reduction in the use of SRAM-based FPGAs. Flash-SRAM hybrid devices are not used as much as flash or SRAM alone, but their satisfaction levels are close to flash. In antifuse markets, more than 85% of respondents expect these FPGAs to stay the same or decrease over the next year.

We asked about IP cores, and discovered that soft microprocessor cores, interface controllers, interface elements, and embedded memory were realms where users expected

usage to increase or at least stay the same. Function-specific blocks, hard microprocessor cores, video compression blocks, and soft DSP cores also proved popular, but skewed more toward "usage will stay the same." It is interesting to note that wireless interfaces had fewer users expecting increased usage, which may indicate saturation in wireless markets. This is true somewhat for hard DSP cores as well, though that could indicate that users prefer soft MAC and vector functions for imaging and signal processing.

In embedded processors for FPGAs, the PowerPC is still top dog, at 64.5% in commercial designs, 47.9% in military. This is followed by ARM, with 31.6% and 31.8%, respectively. Microblaze and Nios soft cores rank next, in the low 20s, followed by MIPS and Tensilica. When we asked designers what they anticipated using in the future, however, the vendor-specific Microblaze and Nios cores improved, with rankings in the high 20s and low 30s, with ARM in particular and PowerPC as well showing drops in use. PowerPC remained in top place, however.

We asked designers the minimum production volume at which they would consider moving from FPGA to ASIC, and the answer was clear: not until 100 units and above, cited by 80% in both commercial and military environments. Most users expect this minimum production volume to stay the same or increase slightly over the next year. But 55.8% of users did not think it was important for a vendor to provide a clear PLD-to-ASIC migration path, while another 28.5% rated it only "somewhat important."

We asked users which vendor characteristics were most important in choosing an FPGA, and "reliability" ranked on top, with 61.5% calling it very important, and 26.2% calling it critical. Time to market was also called very important by 60%, though fewer called it critical. Other high-ranking criteria included available staff, quality of EDA tools, risk of design failure, and risk of verification failure. We learned that overall performance, unit costs, and NRE costs were important, but not quite as critical as the above criteria. For all the talk of power management, power dissipation also ranked only mildly important.

The reason Xilinx dominates brands mentioned by users is explained in part by market share. More than 80% of respondents reported using Xilinx FPGAs, followed by Altera (58%), Actel (26%), Lattice (26%), Cypress (18%), Atmel (14%), and QuickLogic (6%). Consequently, Xilinx ranked at the top in nearly all dimensions, usually 20 percentage points or more ahead of Altera, which itself stayed consistently ahead of Actel and Lattice.

We mentioned exceptions to this rule earlier on, in the cases of military radiation-induced upsets, and power dissipation. Actel also moved into an 18% position among mil-aero responders on the dimension of "risk of verification failure." Xilinx tied for first with Altera on

unit costs, with both ranked at 37%. Military users ranked Actel second in lowest power dissipation, at 28% compared to Xilinx's 32%.

ANALOG COMPONENTS

Our survey was dominated by those who specify less than $50,000 of analog components per year (41.1%), though the rest of respondents were distributed evenly across several categories, including 11.1% specifying $1 million or more per year. An equally wide distribution is seen in number of components specified per year, going from 1 to 5, to more than 100. Designers' products have relatively long lifetimes, with more than 50 percent in aggregate reporting lifetimes of either 5 to 9 years, or 10 years or more – in both commercial and military realms.

Analog respondents predominantly came from mil-aero and industrial, with a smattering from consumer electronics and a surprisingly low percentage from the PC/peripherals world. When asked to name the three most important criteria for analog, specifications and quality beat out prices (75.2% and 54.1%), though prices came in third at 45.%. Other important criteria were delivery and overall system cost. The availability of a second source is considered very important by 37.5% and somewhat important by 45.5%. Analog vendors may not have to worry about reduced supplier lists – 64.5% thought that the number of vendors they work with would stay the same, while 27.2% thought they would increase somewhat.

In vendors cited, Analog Devices played almost as dominant a role as Xilinx in FPGAs – though Texas Instruments and National Semiconductor beat ADI on price competitiveness. Along most dimensions, ADI was in first place, followed by TI, with Linear Technology and National battling for third and fourth position. In most domains such as on-time delivery, product performance, and application support, ADI held a lead in the 80-percentiles, with TI following in the 40s or 50s. It is interesting to note that Linear's 47.6% ranking on product performance moved the vendor into second place in mil-aero accounts, and its 49.8% ranking was very close to TI's in commercial accounts.

MILITARY-AEROSPACE-SPECIFIC QUESTIONS

In addition to the mil-aero rankings listed above, AFRL (FMAC) defined questions specific to this audience, which was dominated by applications in signal processing (31.8%), avionics (28.7%), and space-borne applications (17.8%). Some 58% of respondents had to deal with single-event upsets. Among specialized problem sets this group had to deal with, the most commonly mentioned were memory management, hard embedded processors, floorplanning

of designs, and power management. When asked about an open-source Linux ported to a PowerPC, 51.3% would find it very useful, and another 18.8% would find it somewhat useful.

AFRL's FMAC has been looking at certification programs for engineers. Some 32.3% still find it not necessary, but 31.3% would like to see certification for a specific program. Nevertheless, 68% said their organization would give preference to an engineer certified as "good."

We asked if users would be interested in a universal scrubber that could fix configuration faults. Some 60% said they would be interested, and 70% said it would not be important to be open source. The scrubber would be more important in saving time to market than NREs, and users said they'd prefer to see a parasitic scrubber (one per FPGA) than a daisy-chained device. Other special FPGA features users would like to see include hardened clocks, hardened FIFOs, and guarded I/O.

Some 52 percent of users have special needs going beyond terrestrial and commercial requirements, such as auto-restart, TMR, and rollback. We found significant interest in a new tool that could read EDIF input and translate it into a circuit model. Almost all users expressed at least some interest in a tool that could explore EDIF models for problems such as unprotected cross-sections and sensitivity to faults.

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This survey was conducted by EE Times in collaboration with COSMIAC
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