JVSTB
Journal of Vacuum Science & Technology B

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Citation: Journal of Vacuum Science & Technology B **32**, 011205 (2014); doi: 10.1116/1.4837436
View online: http://dx.doi.org/10.1116/1.4837436
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Direct evidence for interface state annealing in the negative bias temperature instability response

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(Received 16 July 2013; accepted 15 November 2013; published 4 December 2013)

Using a rapid data acquisition methodology, the authors examine the time dependent recovery of the "permanent" component of charge build-up due to the negative bias temperature instability in Si based p-channel field effect transistors in inversion and n-channel devices in accumulation. The authors find clear evidence for recovery of the charge associated with interface states for elevated temperatures (≥150 °C) and for extended times ($t_{recover} \sim 20\,000$ s). Recovery appears to begin at shorter times for p-channel devices than for n-channel. An explanation is advanced both for the mechanism of interface state annealing and for the difference observed between p and n channel devices. © *2014 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4837436]

I. INTRODUCTION

Despite significant research into the negative bias temperature instability (NBTI) phenomenon,[1–3] many questions remain as to its exact physical nature. Evidence has been provided for at least three unique contributions to NBTI in p-channel (PMOS) metal-oxide-semiconductor field effect transistors (MOSFETs) and two in n-channel (NMOS) MOSFETs.[4] In the former case, gate oxide insulator related charge trapping defects, which discharge rapidly[5,6] after bias stressing is removed, are identified with near interface oxygen vacancy centers[7] [recoverable charge (RC)]. Other traps associated are with electrical dipoles (switching traps[8]), which are assumed to commute between +q and 0 charge states under the application of a small positive electric field in the gate insulator following initial electrical stressing. These have been termed field recoverable charge (FRC) since their charge state can be reversed dependent upon the sign of the recovery field and because we have no spectroscopic evidence that the defects are identical to those identified as and termed[8] switching traps. Finally, it is well documented[9] that interface states (IS) also result from NBTI. As indicated above[4] in p-channel devices, we have observed RC, FRC, and IS while in n-channel devices, we have detected only FRC and IS. Extensive debate exists on the nature of annealing of the so-called "permanent" component of NBTI.[10] Initial studies[11] were interpreted as indicating that both the bias stressing induced threshold voltage shift (ΔV_{th}) and an observed recovery were associated with IS. However, the demonstration of the existence of RC and FRC as well as IS suggests this identification may have been premature. Detailed studies[10] of recovery "plateau" have been interpreted as contributions from IS and donor-like switching traps present in the oxide which could coincide with what we have termed FRC.

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In this article, we report the results of a study in which we have endeavored to isolate only the NBTI induced IS component of ΔV_{th} and observed its temperature dependent growth and recovery. We discuss an annealing mechanisms that are consistent with models previously suggested,[12,15] to explain the origins of NBTI.

II. EXPERIMENTAL PROCEDURE

PMOS and NMOS devices were used in the experiments reported here: the nominal channel lengths were 130 nm, channel widths, 5 μm, and 3.4 nm thick silicon oxynitride gate insulators. Measurements were carried out at various temperatures up to 220 °C; however, generally the n-channel devices in accumulation did not tolerate extended stressing at high temperature so we limited our measurements of them to 180 °C. A Keithley Instruments Inc. 4200-SCS semiconductor characterization system was used to acquire data. In order to electrically stress the devices (p or n channel), pulses of amplitude V_{gs}(stress) were applied to the gate contact. No specific V_{gs}(stress) study was undertaken here although various amplitudes were used in an effort to obtain a maximum NBTI effect. For the p and n-channel devices we will report, a pulse of magnitude $V_{gs}(\text{stress}) = -3.25$ V and 3.5 V, respectively, was typically applied between the gate contact and the shorted source/drain/body contacts of the device. The respective oxide electric fields were then 7.9 MV cm^{-1} and 8 MV cm^{-1} as determined using the SILVACO ATLAS™ software to model the devices. With this V_{gs}(stress), we had essentially the same stressing field in the gate dielectric even though the p-channel devices were in inversion and the n-channel in accumulation. A pulse repetition frequency of 10 kHz was used together with a duty cycle of 10%. Each pulse therefore consisted of a 10 μs stress component plus a 90 μs "recovery." During the recovery, a V_{gs} of +1.5 V was applied, which we have previously ascertained,[4] was adequate to remove any remnant FRC or RC

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related trapped charge, thus leaving only the component of ΔV_{th} associated with IS. Other authors[5,6] have discussed the charge detrapping kinetics of RC and demonstrated that recovery in the presence of an oxide field is accelerated. To our knowledge, no such modeling exists for the FRC component. The method of determination of $\Delta V_{th}(IS)$ has been described in detail previously, but will briefly be recalled for completeness. Initially, a source–drain current (I_{ds}) curve as a function of gate–source voltage, V_{gs}, was determined in the linear regime[13] ($V_{ds} \sim -50$ mV for the p-channel device and 50 mV for the n-channel) and the measurement value of V_{gs} ($V_{gs,m}$) established at $dI_{ds}/dV_{gs}|_{max}$. In the usual way,[13] V_{th}° was determined by extrapolation of a line of slope $dI_{ds}/dV_{gs}|_{max}$ to the V_{gs} axis touching the I_{ds} curve at the point of maximum slope. Following any given stress sequence we determined $\Delta V_{th}(IS)$ using the formula $I_{ds} = k[V_{gs,m} - V_{th}^{\circ} - \Delta V_{th}(IS)]$, where k is a constant. For our measurements, the time to acquire a single point $I_{ds}(V_{gs,m})$ was $\sim 4\,\mu s$. Following application of the pulsed stress for a total of 2000 s (corresponding to an actual stress time of 200 s), recovery was allowed with the source/drain and body contacts shorted and $V_{gs} = 0$ V. Periodically, the positive voltage was removed, and $\Delta V_{th}(IS)$ determined from a spot measurement of I_{ds} at $V_{gs,m}$. This process was carried out for a maximum recovery time of 3000 s except for certain cases where the time was extended to 20 000 s.

III. RESULTS AND DISCUSSION

In Figs. 1 and 2, we show the bias stress induced growth of the threshold voltage shift due to interface state generation [$\Delta V_{th}(IS)$] at various temperatures for PMOS and NMOS, respectively. NBTI induced hole trapping at RC and FRC defects induces a negative variation of $\Delta V_{th}(IS)$, both for n- and p-channel devices. Interface state generation, however, results in a positive $\Delta V_{th}(IS)$ for NMOS devices and a negative value for PMOS. The opposite sign behavior shown in Figs. 1 and 2 therefore provides some supportive evidence for our contention that our stressing methodology indeed generates interface states. Furthermore, if one takes the experimental data for the two types of devices at 120 °C, and fits the curves using a law of the form:[1] $\Delta V_{th}(IS) = At_{stress}^{\alpha}$, where t_{stress} is the total stress time then one obtains the curves shown in Fig. 3. Similar fitting was performed for 150 °C and 180 °C data (not shown). All of the data sets can be fitted with $\alpha \sim 0.3$, although the A values are different. This latter fact is not necessarily surprising for two reasons. First, we anticipate A will contain some Arrhenius term, and second, one must bear in mind the fact that the PMOS is stressed in inversion while the NMOS is in accumulation. It is also interesting to note that the PMOS data in Fig. 1 (where we were able to extract data for T > 180 °C) indicates that as the temperature is increased, $\Delta V_{th}(IS)(t_{stress})$ does not increase monotonically with temperature but actually decreases. For example, comparing $\Delta V_{th}(IS)$ at 200 s for 220 °C and 180 °C, we observe that the former is smaller than the latter. We believe this is the first indication in our data that some form of annealing of interface states is occurring. Similar effects have been noted[14] in the radiation induced growth interface states.

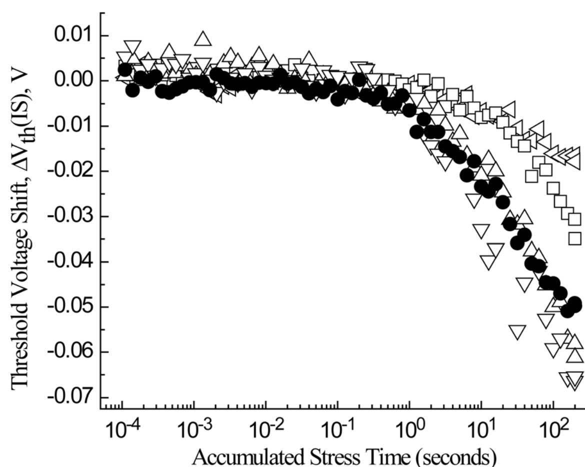

FIG. 1. Bias stress induced growth of the threshold voltage shift due to interface state generation in PMOS for multiple temperatures: 120 °C (◁), 150 °C (□), 180 °C (△), 200 °C (▽), and 220 °C (●).

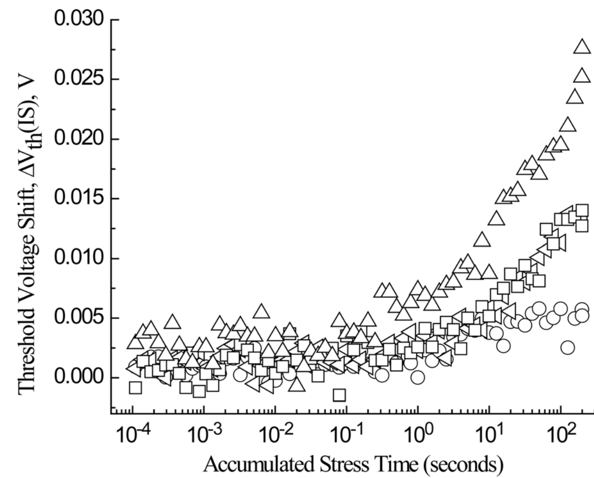

FIG. 2. Bias stress induced growth of the threshold voltage shift due to interface state generation in NMOS for multiple temperatures: 90 °C (○), 120 °C (◁), 150 °C (□), and 180 °C (△).

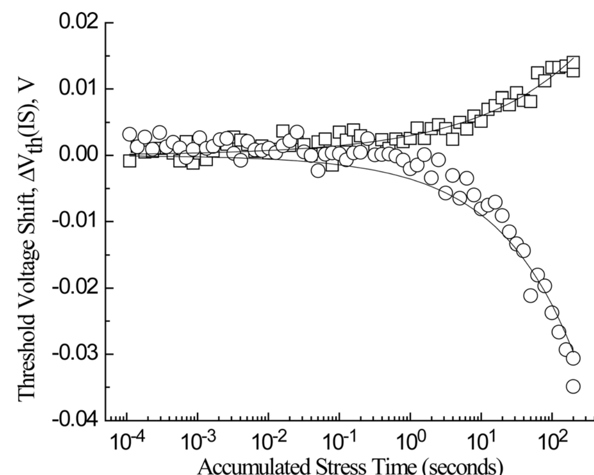

FIG. 3. Measured growth of the interface state term and fitted form of $\Delta V_{th}(IS) = At_{stress}^{\alpha}$ at 120 °C for PMOS (○) and NMOS (□).

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Finally, in Fig. 4, we show the behavior of $\Delta V_{th}(IS)$ measured following the end of 200 s of stressing then allowing recovery at $V_{gs} = 0$ V for various temperatures. In general, recovery was allowed for 3000 s, although for certain temperatures times up to 20 000 s were studied. We see that for both NMOS and PMOS devices for temperatures above $\sim$150 °C, the recovery curve shows an evident reduction in $\Delta V_{th}(IS)$ with recovery time. This effect is more visible for the PMOS than for the NMOS. Furthermore, $\Delta V_{th}(IS)(PMOS)$ appears to begin decreasing for times $\geq$1 s whereas for the NMOS recovery is after $\sim$100 s. The data shown in Figs. 1 and 4 are indicative of the presence of some form of annealing/back reaction in the generation of interface states as can be demonstrated with a simplified argument. We consider some form of simple first order equation[15] for the rate of change of the density of interface states, N_{it}

$$dN_{it}/dt = k_F(N_{it}{}^{o} - N_{it}) - k_R(N_{it}), \tag{1}$$

where $N_{it}{}^{\circ}$ is the maximum density of interface states available. k_F and k_R are forward and back reaction coefficients. Solution of Eq. (1) yields

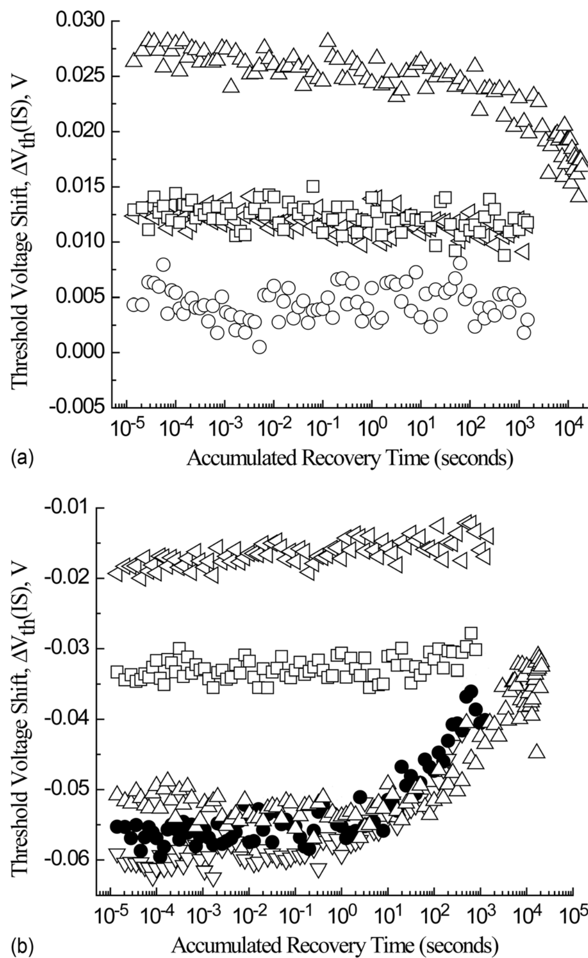

FIG. 4. Evidence for annealing during recovery of $\Delta V_{th}(IS)$ in PMOS (a) and NMOS (b) for different temperatures including: 90 °C (○), 120 °C (◁), 150 °C (□), 180 °C (△), 200 °C (▽), and 220 °C (●) after 200 s of stress for $V_{gs} = -3.25$ V for PMOS and $V_{gs} = -3.5$ V for NMOS.

$$N_{it} = k_F N_{it}{}^{o}(1 - e^{-(k_F + k_R)t})/(k_F + k_R). \tag{2}$$

Examination of Eq. (2) shows that if k_R is small with respect to k_F then the saturation value of N_{it} $(N_{it,sat}) \sim N_{it}{}^{\circ}$ and the effect of k_F is to change the rate at which one tends to the saturation value. If we now suppose k_R increases with increasing temperature then $N_{it,sat} = k_F\, N_{it}{}^{\circ}/(k_F + k_R)$, which is smaller than for the case of a forward reaction alone. Therefore, we can expect that the variation of $\Delta V_{th}(IS)$ with time shows a maximum as a function of temperature as shown in Fig. 1. We underline the fact that we are presenting a plausible argument, not an exact scientific explanation. The nature of the forward and back reactions remains to be discovered though it seems most likely that they result from a complex sequence of processes.

The annealing curves shown in Fig. 4(a) were generated for PMOS [negative $\Delta V_{th}(IS)$] and Fig. 4(b) for NMOS devices [positive $\Delta V_{th}(IS)$] by stressing for 200 s at various temperatures then allowing recovery at those same temperatures with $V_{gs} = 0$ V. It is interesting to note that for both types of devices, there is little observable recovery (up to 3000 s) for $T < 150$ °C whereas for $T > 150$ °C, there is recovery and this is more obvious in the case of PMOS than in NMOS. In order to understand Fig. 4, it is necessary to examine the experimental methodology. Taking the PMOS case as an example during the annealing phase, under small positive bias, the RC traps are empty, and the FRC traps in a neutral dipole state. Excess interface states generated during NBTI stressing would be in the neutral dangling bond state $Si_3{\equiv}Si^{\bullet}$. V_{gs} is then switched in $\sim$20 ns to $V_{gs,m} \sim -0.5$ V and the source–drain current measured (I_{ds}), the dangling bond centers then take on a charge consistent with the PMOS or NMOS nature of the device ($Si_3{\equiv}Si^{\pm}$). Returning to the annealing condition eliminates the charge and returns the dangling bond to its neutral state. Therefore, we suggest that the observed interface state annealing shown for both NMOS and PMOS in Fig. 4 is true annealing in the sense that it actually results from repassivation of neutral Si dangling bonds generated during the NBTI stressing process

$$Si_3 \equiv Si^{\bullet} + X \rightarrow Si_3 \equiv Si{-}H + Y, \tag{3}$$

where X and Y are species/reaction products yet to be identified. A cautionary identification of X can be made. Temperatures $\sim$150 °C may be too low to reasonably suggest that H_2 dissolved in the gate dielectric is involved as it is in the classical technological passivation step with an activation energy $\sim$1.6 eV, which may be too large.[16] We therefore recall that it is known[17] that atomic hydrogen can spontaneously passivate $Si^{\bullet}$ and it is known that dopant-hydrogen complexes present in Si substrates can release atomic H at low temperatures.[12] We suggest that this may be a possible source of atomic H required to explain the anneal data in Fig. 4.

IV. SUMMARY

NBTI pulsed stressing has been carried out on NMOS devices in accumulation and PMOS in inversion at different

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temperatures up to 180 °C (NMOS) or 220 °C (PMOS) to allow direct measurement of the interface states. Following stressing, the devices were annealed at the stressing temperatures at zero bias. Using an anneal/measure/anneal procedure, annealing curves were generated. In both PMOS and NMOS devices, we observed evidence for passivation of neutral dangling bond defects. We attribute this passivation to atomic hydrogen released from dopant-H complexes in the n and p type substrates although the possibility of passivation through dissolved H_2 cannot be totally excluded. Evidence for some form of annealing was also observed in the measured interface state density growth as a function of NBTI stress time/temperature though the physical nature of this may be more complex than for the case of the pure annealing curves. This data is consistent with temperature dependent behavior observed in the generation of interface states in prompt ionizing radiation experiments.

ACKNOWLEDGMENTS

The authors gratefully acknowledge correspondence with Tibor Grasser, Ph.D., of the Technical University of Vienna, Austria. The work performed by D.D.N. and C.K. is based on research sponsored by the Air Force Research Laboratory under agreement number FA9453-08-2-0259. The work performed by K.E.K. was supported by the US Air Force under contract FA9453-08-C-0245 sponsored, monitored, and managed by: United States Air Force Air Force Material Command, Air Force Research Laboratory, Space Vehicles Directorate, Kirtland AFB, NM 87117-5776.

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