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Extraction of recoverable and permanent trapped charge resulting from negative bias temperature instability

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We have studied defect charging and discharging resulting from negative bias temperature instability in nitrided SiO_2 gate insulator field effect transistors. Using pseudo-DC and pulsed stressing methods, we are able to extract at least three individual components associated with a) interface states at the semiconductor/insulator boundary, b) dynamically recoverable positive charging in the "bulk" of the insulator, and c) positive charge in the insulator which can be "eliminated" by application of a positive electric field across the insulator. It is argued that the charge variation in c) in fact arises via a charge neutralization process involving electron capture at switching traps and that this process can be simply reversed using a small negative field. The important role played by neutral oxygen vacancies (O_3≡Si-Si≡O_3) and/or their variants involving partial N substitutions is emphasized.

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1 Introduction

The negative bias temperature instability (NBTI) is a phenomenon occurring in p-channel metal-oxide-semiconductor field effect transistors (MOSFETs). Under normal operation [1] a negative potential is applied to the gate contact with respect to the source terminal, and an inversion layer (holes) is induced in the area immediately under the gate insulator in the semiconductor bulk. It has been observed that extended negative biasing in such structures results in degradation of the device working parameters (in particular the threshold voltage, V_{th} [1]), leading ultimately to device/circuit failure. In order to develop predictive models for failure, a deeper physical understanding of the defects involved and their generation kinetics is required. Though it is clearly recognized that NBTI is associated with positive charging at the semiconductor/insulator interface and in the "bulk" of the insulator, there is significant debate [2, 3] as to the physics of the defects involved and the mechanism by which charging or discharging of the defects takes place. Before these problems can be clarified, it is necessary to develop an experimental protocol that will enable independent extraction of the various components of NBTI-induced charging. In the work presented here, we have applied pseudo-DC electrical stressing methods together with a technique in which stress is applied in a pulsed manner with a specifically chosen on/off duty cycle. It is demonstrated that, given certain approximations, this methodology enables access to three components of charging-induced threshold voltage variation: $\Delta V_{th(IS)}$ associated with interface states, $\Delta V_{th(RC)}$ associated with insulator charge which spontaneously recovers by tunnelling from traps into the underlying substrate and $\Delta V_{th(FRC)}$ associated with charges in the insulator which are neutralized under the application of a positive oxide field.

2 Experimental

The threshold voltage is determined in the device's linear regime [1] through measurements of the source-drain current, I_{ds}, as a function of the gate-source voltage, V_{gs}. The source-drain voltage is typically -50 mV. $I_{ds}(V_{gs})$ is expressed as

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$$I_{ds} = (W/L)\mu C_{ox}(V_{gs} - V_{th})\, V_{ds} \quad (1)$$

where W and L are the width and length of the conducting inversion channel, μ is the carrier mobility and C_{ox} is the gate insulator capacitance. For small changes in V_{th}, ΔV_{th}, one can approximate:

$$\Delta V_{th} = (1 - I_{ds}/I_{ds}^{o})(V_{gs} - V_{th}^{o}) \quad (2)$$

where I_{ds}^{o} and V_{th}^{o} are initial (time t = 0) values prior to any NBTI stressing. I_{ds} is the value of the current at V_{gs} following some electrical stressing sequence.

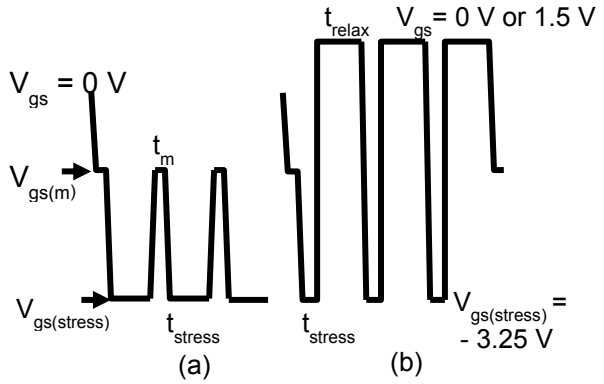

Figure 1 a) The pseudo-DC measurement sequence for V_{gs}. b) The pulsed stress/measurement sequence for V_{gs}.

2.1 Pseudo-DC measurements

These measurements are made following the voltage application schematic shown in Fig. 1a. At time t = 0, the device gate voltage is ramped to the measurement $V_{gs(m)}$ in approximately 20 ns and I_{ds}^{o} is measured. $V_{gs(m)}$ is typically -0.5 V whilst V_{ds} is -50mV. The measurement time is ~ 4 μs. Subsequently, V_{gs} is ramped to the stressing voltage $V_{gs(stress)}$ and V_{ds} is set to 0 V – this stressing condition is maintained for a chosen time, t_{stress}. Following the stress sequence, V_{gs} is reduced to $V_{gs(m)}$ and $I_{ds}(t_{stress})$ determined. The process is repeated, typically starting at stress times ~ 10 μs out to 1500 s. Using Eq. (2), a stress curve $\Delta V_{th}(t_{stress})$ is generated.

2.2 Pulsed measurements

This technique was developed to probe permanent and recoverable components of NBTI. Following the diagram shown in Fig. 1b, a pulsed stress sequence is employed with a duty cycle, D ($0 \le D \le 1$), and pulse repetition frequency, ν. The situation at time t = 0 is analogous to the pseudo-DC case and I_{ds}^{o} is measured. The first stressing pulse is then applied at $V_{gs} = V_{gs(stress)}$ for a time $t_{stress} = D/\nu$, after which $V_{gs(stress)}$ is changed to either 0 V or + 1.5 V, allowing a relaxation to occur (if present). The total relaxation time per pulse sequence is (1-D)/ν. Following Fig. 1b. a measurement of $I_{ds}(t_{stress})$ is made following (t_{real}) ν pulses such that $t_{stress} = D\, t_{real}$. The unique character of the measurement performed is that $I_{ds}(t_{stress})$ is determined immediately following the recovery period at $V_{gs(stress)}$ = 0 V or + 1.5 V of the final pulse sequence i.e. after the ($t_{real}\nu$)'th pulse. Repetition frequencies in the range 1 Hz ≤ ν ≤ 100 kHz were employed in our experiments but no difference in results was observed.

3 Results

All measurements reported here were carried out at 120 °C on 130 nm channel length by 5 μm channel width Si MOSFETs with 3.4 nm thick nitrided SiO_2 gate dielectrics. $V_{gs(stress)}$ was chosen as -3.25 V. For the pulsed measurements, D was optimized to be 0.25 as discussed in Section 3.2.

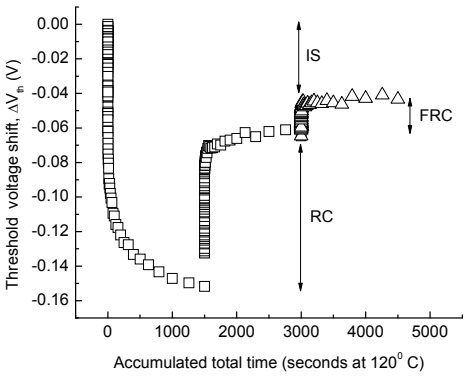

Figure 2 Pseudo-DC stressing data at 120 °C. $0 \le t \le 1500$ s, V_{gs} = -3.25 V; 1500 s ≤ t ≤ 3000 s, V_{gs} = 0 V; 3000 s ≤ t ≤ 4500 s, V_{gs} = 1.5 V.

3.1 Pseudo-DC data

The results of pseudo-DC experiments, using Eq. (2) to convert $I_{ds}(t_{stress})$ into $\Delta V_{th}(t_{stress})$, are shown in Fig. 2.The initial stressing was carried out for 1500 s, then the device was allowed to recover with $V_{gs(stress)}$ = 0 V for 1500 s. As can be seen, ~ 70% of the maximum ΔV_{th} (ΔV_{th}(max.)) resulting from the first 1500 s stress sequence recovers spontaneously even in the absence of a driving electric field (symbolised by RC).

Subsequent application of a positive potential to the gate (V_{gs} = + 1.5 V) induced a further recovery ~6.5% of ΔV_{th}(max.), whilst the remaining 23.5% of ΔV_{th}(max.) did not recover even when the recovery time was extended to 12,000 seconds. The results are consistent with the presence of at least three types of trapped positive charge (leading to negative ΔV_{th} shifts).

There is some question as to the existence of recovery plateaus as shown in Fig. 2 [4] for the RC component. Experiments were done for relaxation times of 12,000 s and no additional recovery was observed.

3.2 Pulsed data

Based upon the pseudo-DC stressing and recovery data presented above, it is clear that relaxation in the presence of a + 1.5 V bias on the gate electrode results in removal of

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all "mobile" charge (or at least the measurable "mobile" charge), leaving only permanently charged defects. We therefore conducted a study in which we applied pulsed stress (Fig. 1b) and varied the duty cycle (D). We observed that a duty cycle of 0.25 was sufficient to ensure that during the +1.5 V part of the pulse recoverable charge was entirely recovered, within experimental accuracy. We therefore performed a stressing experiment on a fresh device using D = 0.25 and $V_{gs(stress)}$ = -3.25 V. The data obtained using a pulse repetition frequency of 10 kHz is shown in Fig. 3. It is interesting to note that the data can be fitted using a power law expansion:

$$\Delta V_{th(IS)} = -0.0058\ t_{stress}^{0.27} \quad (3)$$

where we use the terminology IS to imply interface states, although in fact, some of the permanent charging may result from hole trapping at energetically deep traps in the gate insulator. We note that the pulsed data at 1500 s yields $\Delta V_{th(IS)}$ = - 0.042 V, which agrees very well with the value $\Delta V_{th(IS)}$ ~ - 0.037 V ascertained from the data shown in Figure 2 resulting from the pseudo-DC study.

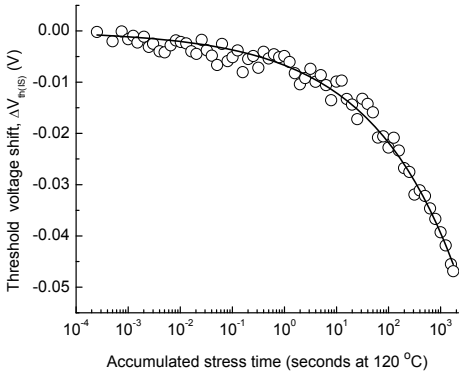

Figure 3 $\Delta V_{th(IS)}$ (t_{stress}) determined using the pulsed stress method described. The line shows the fit using Eq. (3).

3.3 Cyclic recovery data

The data, shown in Figure 2 and confirmed by that in Fig. 3, indicates that application of a positive gate bias during the recovery phase removes all measurable "mobile" charge. We have ascertained that for our case + 1.5 V was adequate. However, this begs the question as to whether all the mobile charge has been removed or only the measurable charge, so to clarify this, we performed a series of cyclic bias experiments. A device was stressed for 1500 s with $V_{gs(stress)}$ = -3.25 V then allowed to relax with $V_{gs(stress)}$ = 0 V. Subsequently we applied first + 1.5 V for 500 s followed by -1 V for 500 s; this (+ 1.5 V/-1.0 V) cycle was repeated five times. The variation, which we call $\Delta V_{th(FRC)}$, symbolises a field recoverable charge component that can be recovered and "discharged." The cyclic behaviour of $\Delta V_{th(FRC)}$ is shown in Fig. 4; the maximum excursion appears to be ~ -0.02 V.

4 Discussion

On the basis of the data shown in Figs. 2, 3 and 4, we propose that NBTI in our nitrided SiO_2 gate insulator devices provides evidence for at least three types of defect-related positive charge trapping. These result in independent threshold voltage shift components, $\Delta V_{th(IS)}$, $\Delta V_{th(RC)}$ and $\Delta V_{th(FRC)}$. We have reasoned that the data in Fig. 3 represents $\Delta V_{th(IS),}$ which may be comprised of positively charged interface states and positive trapped charge in the gate insulator that does not spontaneously relax or relax under a positive oxide field. We have performed analogous pulse experiments (not shown) to those used to determine Fig. 3 but in which the baseline of the pulse was

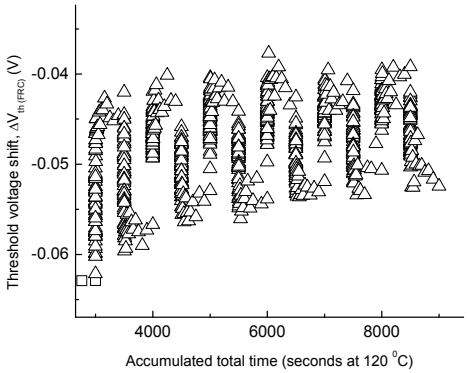

Figure 4 Oscillatory behaviour of $\Delta V_{th(FRC)}$ following stressing for 1500 s at -3.25 V then relaxation (1500 s) under 0 V bias (Fig. 2) then cycles of V_{gs} = 1.5 V followed by V_{gs} = -1 V.

0 V as opposed to + 1.5 V. This data allows us to extract ($\Delta V_{th(IS)}(t_{stress}) + \Delta V_{th(FRC)}(t_{stress})$) so that, by subtraction of $\Delta V_{th(IS)}$ determined from Fig. 3, we can deduce $\Delta V_{th(FRC)}(t_{stress})$. Having deduced two of the three threshold shift growth terms, we can obtain the third, $\Delta V_{th(RC)}(t_{stress})$, using the data from Fig. 2 together with $\Delta V_{th(FRC)}(t_{stress})$ and $\Delta V_{th(IS)}(t_{stress})$ by subtraction. We show the estimated growth curves under the conditions of our experiments in Fig. 5.

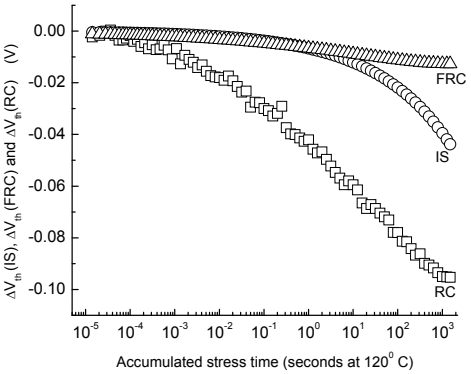

Figure 5 Electrical stressing induced growth curves for the three NBTI components: $\Delta V_{th(IS)}$ from permanent interface states, $\Delta V_{th(RC)}$ from tunnelling charged traps, $\Delta V_{th(FRC)}$ from switching traps.

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As mentioned previously, there continues to be significant debate about the physics of interface state generation during NBTI [2,3,5]. It was assumed that the simplified interaction of a hole from the conducting inversion layer with an interfacial passivated dangling bond resulted in

$$\text{Si-H} + h^+ \rightarrow \text{Si}^+ + \text{H}. \quad (4)$$

However, this turns out to be energetically unfavourable. Furthermore, based upon this and the reaction-diffusion (RD) model [2], it is assumed that there is a forward, interface state generation term (Eq. (4)) and a reverse, annealing term associated with the concentration of H or H_2. The latter was presumed to account for the observed annealing in $\Delta V_{th(IS)}(t_{stress})$. However, radiation induced interface states arising from the generation of H^+ in the dielectric and trapping at the interface

$$\text{Si-H} + H^+ \rightarrow \text{Si}^+ + 2\text{H} \quad (5)$$

(where 2H may be two H atoms or the dimerized H_2 molecule) do not show evidence for substantial annealing at the temperatures where we have studied NBTI [5,6]. We find no evidence of annealing of the $\Delta V_{th(IS)}$ component. We do, however, note that the RD model predicts a t^{α} variation of $\Delta V_{th(IS)}$ with time and $\alpha(H) \sim 0.25$ and $\alpha(H_2) \sim 0.16$, which are not very different from the value we find of 0.27 (Fig. 3). It must, however, be re-iterated that the term we call $\Delta V_{th(IS)}$ here may contain both stable interface states and permanently charged oxide defects and that we are therefore extracting a combined time dependence.

The recoverable charged defect term, $\Delta V_{th(RC)}$ appears to be spontaneously relaxing in the absence of a stressing voltage. This term has been demonstrated to be reversible, although it is assumed that reversibility is by tunnelling [7]. For the case of "pure" SiO_2, it has been suggested that the defects involved in reversible charging/discharging are neutral oxygen vacancies, ($O_3{\equiv}Si\text{-}Si{\equiv}O_3$) so that by trapping a hole it can transform into the positively charged, spin active, E'_{δ} defect [8,9]

$$(O_3{\equiv}Si\text{-}\uparrow\downarrow\text{-}Si{\equiv}O_3) + h^+ \rightarrow O_3{\equiv}Si\text{-}\uparrow\text{-}Si{\equiv}O_3 \quad (6)$$

and the positive charge on the right-hand side is localized on the defect. Energetically, the trapped hole is argued to be shallow [9], so the defect is dynamic and can readily release the trapped hole; it is not therefore bi-stable. Whereas these defects are expected to be numerous in SiO_2, it remains to be determined what happens in nitrided SiO_2 where N incorporation is expected. Experimentally, it would appear that substantial numbers of these dynamic defects remain.

Again by analogy to pure SiO_2, we examine the defects potentially responsible for the cyclic behaviour shown in Fig. 4, $\Delta V_{th(FRC)}$. The defect state can be readily cycled from the +/0 state by application of a small positive V_{gs} value corresponding to an electric field in the dielectric ~ 4.4 MV cm^{-1}. Subsequently, a small negative field ~ -1.7 MV cm^{-1} is adequate to reverse the situation but, from our experiments, is too small to induce the usual NBTI effect by field-assisted tunnelling (as is the case of the dynamic E'_{δ} described by Eq. (7)). This suggests that the positively charged defect, once formed, is not discharged by the positive field but is compensated in the manner of the so called "switching traps" [10] which are assumed to also form from neutral oxygen vacancies:

$$(O_3{\equiv}Si\text{-}\uparrow\downarrow\text{-}Si{\equiv}O_3) + h^+ \rightarrow O_3{\equiv}Si^+ \uparrow Si{\equiv}O_3 \quad (7)$$

$$O_3{\equiv}Si^+ \uparrow Si{\equiv}O_3 + e \leftrightarrow O_3{\equiv}Si^+ \uparrow\downarrow Si{\equiv}O_3 \quad (8)$$

The switching, indicated by Eq. (8), therefore involves compensation. Evidence for this behaviour has been presented for irradiated SiO_2 [11]. It remains to be determined, as for the E'_{δ} situation, whether or not Eqs. (7) and (8) and/or their equivalents in nitrided SiO_2 are justified.

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