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Insight into the multicomponent nature of negative bias temperature instability

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A novel measurement technique is used to extract two physically distinct "permanent" (long lived on our experimental time scale, $\leq$12 000 s) and one recoverable charge components of the negative bias temperature instability in p-channel metal–oxide–semiconductor field effect transistors under inversion and n-channel devices under accumulation. The results suggest that the permanent components are present in both cases, while there is little, if any, recoverable charge present in the case of the n-channel device. A physical explanation is provided involving the band energy diagram to explain these observations. © *2013 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4796115]

I. INTRODUCTION

It is widely accepted that the negative bias temperature instability (NBTI) in p-channel MOSFETs (PMOS)[1,2] results in a threshold voltage[3] shift, ΔV_{th}, which is comprised of at least two terms. These terms are assumed to be associated with positively charged interface states (ΔV_{th}(IS)) and positively charged defects in the gate oxide structure (ΔV_{th}(RC)). The latter are termed "recoverable charge" (RC) because removal of the negative stressing voltage applied to the MOSFET gate results in spontaneous relaxation and disappearance of the ΔV_{th}(RC) component. We have recently reported[4] the results of a study of NBTI using an experimental methodology which allows extraction of the individual components of ΔV_{th} and evidenced a third component which is field recoverable charge, ΔV_{th}(FRC). This component is observed to disappear if relaxation takes place in the presence of a small positive potential but to re-appear if a small negative potential is subsequently applied. The negative potential was not significant enough to generate an NBTI response in itself. The FRC behavior was then associated with switching traps[5,6] in which a trapped positive charge was compensated by a trapped negative charge resulting from electron tunneling in the presence of the positive potential. In the usual model for oxide-related switching traps,[5] both RC and FRC are derivatives of a neutral oxygen vacancy center termed[7] the E′ center. At the present time, it is assumed that the RC component of NBTI is a result of hole tunneling from the PMOS inversion layer into neutral traps located in the gate oxide/dielectric, although the exact location in space/energy is not known. Hole tunneling should also result from accumulation layers in a negatively biased n-channel MOSFETs (NMOS) device although, as shown schematically in Fig. 1, the position in energy of the holes in the silicon valence band should be different, therein enabling a crude form of defect spectroscopy. With this philosophy, we have performed NBTI measurements on n-channel MOSFETs subjected to stress in the accumulation condition then measured in inversion. This work complements a study performed[8] on PMOS and NMOS devices with substantially thicker, pure SiO_2 gate dielectrics. Preliminary results of the study are reported in the following.

II. EXPERIMENTAL PROCEDURE

Both the PMOS and NMOS devices used in the experiments reported here had nominal 130 nm channel lengths, 5 μm channel widths, and 3.4 nm thick silicon oxynitride gate insulators. Measurements were carried out at several temperatures, but only 90 °C data will be shown here. A Keithley Instruments, Inc. 4200-SCS semiconductor characterization system was used to acquire data. Two modes of operation were used.[4] The first corresponded to a "pseudo" continuous stressing mode in which a voltage (V_{gs}) is applied to the MOSFET gate contact with respect to the source and body contacts. At time t = 0 s, the V_{gs} is ramped to some prechosen measurement value ($V_{gs(m)}$) with a rise time of typically 20 ns. At the same time, the source-drain voltage, V_{ds}, is ramped from 0 to –0.05 V (0.05 V for the NMOS), and the source-drain current, I_{ds}, is then measured in an acquisition time window, $\tau_m \sim 4$ μs. This first measurement establishes $I_{ds}^{\circ} = I_{ds}(t = 0\,s)$. The device is then stressed for some chosen time, τ_{stress}, with a gate voltage

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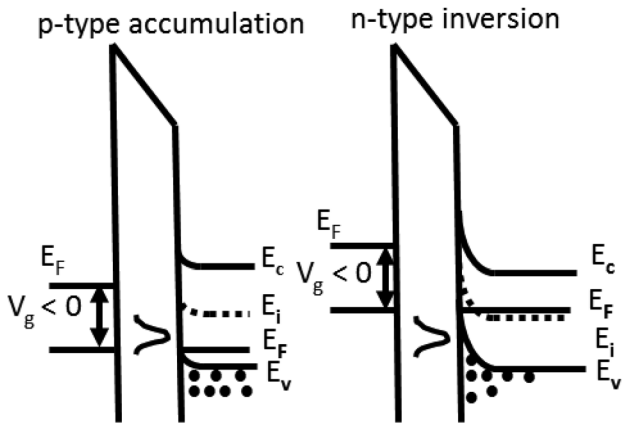

FIG. 1. Schematic representation of the bands for accumulation in an NMOS (p-type substrate) (left) and inversion in a PMOS (n-type substrate) (right). The recoverable charge defects are crudely represented by the distribution shown in the oxide. Note that tunneling of the holes (•) to the defect states is less likely in the NMOS accumulation case than in the PMOS inversion case.

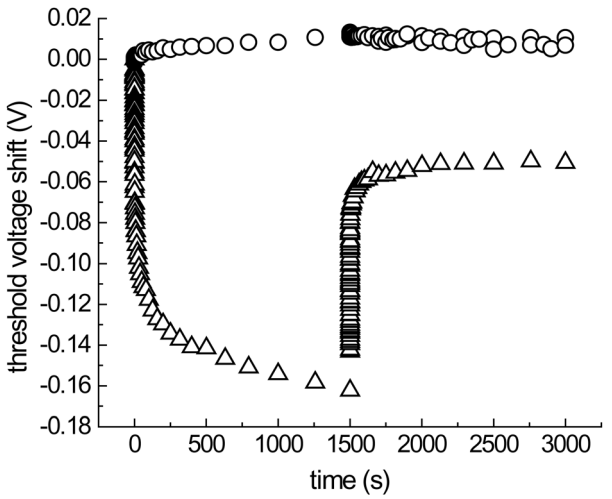

FIG. 2. Measured threshold voltage shift due to NBTI at 90 °C for a PMOS (Δ) and NMOS (O) stressed for 1500 s at $V_{gs} = -3.50$ and -3.75 V, respectively, followed by 1500 s of relaxation at $V_{gs} = 0$ V.

$V_{gs(stress)}$ ($V_{ds} = V_{sb} = 0$ V), after which a measurement sequence is again performed to determine $I_{ds}(\tau_{stress})$. The process is then repeated and the cumulative variation of $I_{ds}(t_{stress})$ (with $t_{stress} = \Sigma\ \tau_{stress}$) determined and converted to $\Delta V_{th}(t_{stress})$.[9] This measurement is analogous to the "on the fly" method where I_{ds} is measured at $V_{gs(stress)}$.[10] However, our approach has the advantage that I_{ds} is measured with $|V_{gs(m)}| < |V_{gs(stress)}|$, which removes a potential source of measurement error.[9]

The second method of stressing uses a pulse stream. In this case, the $V_{gs(stress)}$ applied during the τ_{stress} is a series of stress (τ_{on}) and recovery (τ_{off}) pulses with a duty cycle $D = \tau_{on}/(\tau_{on} + \tau_{off})$. With the system available, a measurement was made at $V_{gs(m)}$ immediately following a τ_{off} recovery period. The total stressing time, t_{stress}, was $N\tau_{on}$, where N was the number of pulses. During the final τ_{off} part of each pulse, dynamic or recoverable charge detrapping can occur. If this time is long enough, the influence of $V_{gs(stress)}$ on the I_{ds} measured corresponds only to that part associated with "permanent" charge trapping. For these experiments, D = 10% is chosen following a series of short stress time experiments (<0.01 s) in which permanent charge trapping was estimated to be small in order to see if there was a buildup of recoverable charge after repeated cycles. Similar testing demonstrated that the use of $V_{recovery} \geq 1$ V during the 90% of the pulse time allocated to recovery resulted in full relaxation of the FRC and RC terms. This approach provides a direct method for determination of the permanent interface charge trapping independently of any recoverable part.

III. RESULTS AND DISCUSSION

The charging due to the application of −3.50 V stressing for 1500 s followed by 1500 s of relaxation at 0.0 V is shown (Δ) for the PMOS studied at 90 °C in Fig. 2. (This represents customary accelerated stress testing for NBTI, necessary to obtain voltage shifts large enough to measure experimentally in a physically acceptable time frame. The relative importance of the individual components will clearly depend on their respective field and temperature dependencies. This variability is presently being studied.) Conversion of the measured variation of I_{ds} into the presented parameter ΔV_{th} was performed using different methods, including the linear approximation[7]

$$\Delta V_{th} = (1 - I_{ds}/I_{ds}^{\circ})(V_{gs(m)} - V_{th}^{\circ}), \quad (1)$$

in which $V_{gs(m)}$ is the measurement voltage, V_{th}° is the pre-stress threshold voltage and I_{ds}° is the source-drain current at time t = 0 s. Typically, $V_{gs(m)} = -0.52$ V and $V_{th}^{\circ} \sim -0.40$ V for the PMOS and $V_{gs(m)} = 0.52$ V and $V_{th}^{\circ} \sim 0.38$ V for the NMOS.

The appropriate bias to correspond to the same oxide field is a subject of some disagreement. However, based on the work of Schroeder[10] and simulations performed using the Silvaco Atlas™ device simulation code, an NBTI bias for the NMOS of −3.75 V was chosen (corresponding to −3.50 V for the PMOS). The results for ΔV_{th} as a function of time for 1500 s of bias stress followed by 1500 s of relaxation at 0 V are shown in Fig. 2. The (O) symbols apply to the case of the NMOS and the (Δ) to the PMOS.

The most striking difference between the PMOS and NMOS results is the absence of any appreciable RC term for the NMOS. This suggests that, as indicated in Fig. 1, the RC-associated traps must be energetically unfavorable for hole tunneling from the accumulation layer in the case of the NMOS but favorable for tunneling from the inversion layer in the PMOS. To reiterate, it can be seen in the schematic band diagram that for both cases, the surface potential, or band bending, in the inversion channel is much larger than the corresponding potential in the NMOS in accumulation. This means that typically only traps within ~0.2 eV of the Si valence band energy can be reached in the accumulation device, while the device in inversion can access traps substantially higher than the valence band energy. The absence of RC component associated with the NMOS in accumulation leads one to question if the FRC component is also absent.

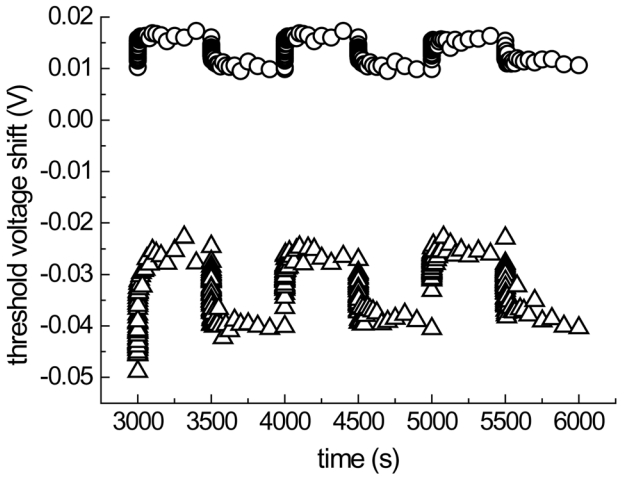

FIG. 3. Measured threshold voltage shift at 90 °C for a PMOS (Δ) and NMOS (O) for oscillating positive (+1.5 V) and negative (−1.0 V) gate biasing following the 1500 s of stress and 1500 s of relaxation shown in Fig. 2.

We recall that initial identification[5,6,11] of the origin of FRC switching traps and RC traps was as derivatives of the E′ oxygen vacancy center. One might therefore expect the FRC component to be also absent in the NMOS case. To address this, a 500 s stress at +1.5 V followed by further stress at −1.0 V was applied immediately following the stress and relaxation sequence shown in Fig. 2. The results are shown in Fig. 3 for both PMOS and NMOS. Whilst there is a difference in the magnitude of the FRC component between the two (20 and 8 mV respectively), the behavior is qualitatively similar, caused by permanent trapped positive charge in the oxide. However, we know that that there is a net positive threshold voltage shift in the NMOS due to negatively charged interface states (see Fig. 4) dominating the FRC component. Based on these observations, we conclude that there is no justification for the hypothesis that the traps resulting in FRC are in any way correlated with those responsible for RC traps.

We have hypothesized that one can independently measure the interface state related ΔV_{th}(IS) component of ΔV_{th} using an alternating stress with a duty cycle of 0.1. These

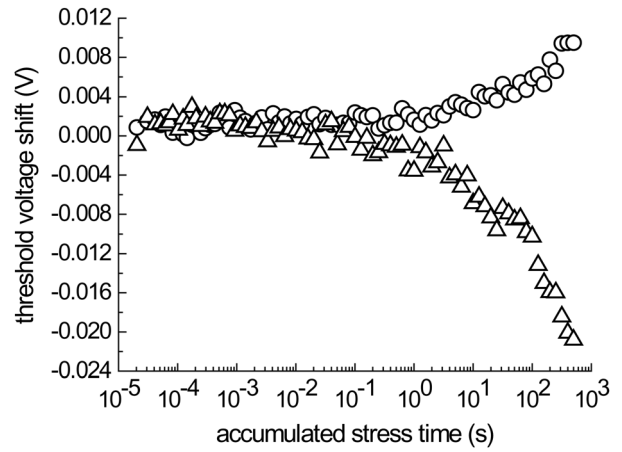

FIG. 4. Measured IS component of the threshold voltage shift at 90 °C for a PMOS (Δ) and NMOS (O) as a function of accumulated stress time.

measurements were performed for both the PMOS and NMOS with stressing at −3.50 and −3.75 V, respectively, and recovery at 1.5 V for a total stressing time of 1000 s. (The total measurement time was 10 000 s.) The results are shown in Fig. 4. The positive threshold voltage shift for the NMOS case and negative shift for the PMOS are consistent with radiation data on NMOS and PMOS devices,[12] where it has been argued that holes in both cases generate neutral interface states. The position of the Fermi level during measurement of the device source-drain current during operation, above Si midgap for the NMOS and below midgap for the PMOS, leads to negative charging of the interface in the former (ΔV_{th}(IS) positive) and positive (ΔV_{th}(IS) negative) in the latter. It remains to explain the nature and generation mechanism of the interface states which become charged during the measurement phase. Various authors have proposed models for interface state generation, including strained interfacial bond rupture[13] and proton assisted depassivation of dangling bonds at the interface.[7] From our experiments, we are unable to resolve this dilemma. However, we note that the neutral dangling bond, $Si^{\bullet}$, is an amphoteric trap usually termed a P_b center which can therefore appear negative in an NMOS and positive in a PMOS. Following other authors, the threshold voltage shifts in Fig. 4 were fitted to a power law[1,2]

$$\Delta V_{th} = A\, t^{\alpha}, \tag{2}$$

where $A = -0.0020 \pm 0.0002$ V and $\alpha = 0.38 \pm 0.02$ for the PMOS and $A = 0.0025 \pm 0.0001$ V and $\alpha = 0.19 \pm 0.01$ for the NMOS.

IV. SUMMARY

We have performed NBTI measurements on both NMOS and PMOS devices. Our results clearly indicate that the PMOS biased in inversion has at least three positively charged defects: recoverable charge associated with oxide traps, interface states, and field recoverable charge. In NMOS devices, we observe positively charged field recoverable charge and negatively charged interface states. Recoverable charge is absent in the NMOS case. This result suggests that FRC and RC traps do not have a common origin but that interface states and FRC may in fact be linked.

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