On the Nature of "Permanent" Degradation in NBTI

D. D. Nguyen and C. Kouhestani
COSMIAC
Albuquerque, NM, USA

K. E. Kambour
Leidos
Albuquerque, NM, USA

R. A. B. Devine
Think-Strategically
Albuquerque, NM, USA

***Abstract*—This paper reports new high temperature measurements of Negative Bias Temperature Instability induced interface states in both NMOS and PMOS devices. Evidence of annealing of the interface states, previously thought to be "permanent", is presented for measurements including a methodology which allows the direct measurement of the time dependent growth/recovery of the interface state component.**

Keywords—NBTI, defects, reliability

I. INTRODUCTION

Field effect transistor dimensions are shrinking and their number per micro-processor is increasing. Coincidentally with this, the overall circuit reliability lifetime is expected to decrease [1]. This is primarily because, to first order, the mean time to failure of a complex circuit is $\propto 1/N$, where N is the number of devices in the circuit. Examination of the predictions of the failure of standard commercial circuits [2] confirms that we are rapidly approaching lifetime limits < 5 years. It is clear, that with existing electronic degradation, it is doubtful whether or not the required 10 – 15 year radiation/reliability hard lifetimes for space based electronics will be met. A secondary reliability related problem, common to both commercial and military application parts, concerns the methodology that must be implemented if we are to measure/model the lifetime of circuits manufactured for long term operation. For space based applications, this problem was less relevant when radiation effects were the dominant cause of circuit failure (with electronic reliability of no concern) and accelerated testing could be performed using high dose rate sources [3]. Clearly, as the reliability lifetime is nearing the radiation induced failure lifetime, a new approach must be found.

What is presently required, then, is a circuit lifetime modeling capability which will enable us to predict lifetimes and test the importance of the various physical mechanisms leading to reliability failure. There are a variety of degradation mechanisms held responsible for individual device failure as enumerated in various technical reviews and reports [1, 2, 4]. In this work we have focused on one specific mechanism, Negative Bias Temperature Instability (NBTI), recognized as being of primary importance in device degradation [5]. Our goal is to elucidate the intrinsic nature of NBTI, and hopefully from that learn what primary factors control it. In this context, we have previously [6] found evidence that at least three components are active in NBTI in our devices and these contribute to the individual device degradation primarily in the form of a threshold voltage shift, ΔV_{th} [7]. These include threshold voltage shift due to recoverable charge (ΔV_{th}(RC)), electric field recoverable charge (ΔV_{th}(FRC)) and interface states (ΔV_{th}(IS)) [6].

At the present time, it is assumed that the RC and FRC components are associated with gate insulator-related trapped charges at defect centers starting life as some form of neutral oxygen vacancy center [8]. The former (RC) recovers when the electrical stress is removed and positive charge tunnels from the oxide traps into the Si substrate. The latter (FRC) has been argued to be trapped positive charges at some form of oxygen-vacancy center which becomes a neutral dipole if a small positive bias potential is applied following the NBTI stress – one form may be a version of the switching traps [9]. These defects are assumed not to recover their initial neutral oxygen-vacancy form by release of their trapped positive charge because of some network relaxation associated with their initial charge trapping. Once the latter components disappear during biased recovery, the remaining "permanent" defects are revealed. The immediate question which arises concerns the nature of the defect we consider to be "permanent" (at least permanent within the range of experimental measurement): Do they actually anneal and is there a simple approach to obtain supporting evidence [10]?

In this work, we demonstrate clear evidence for an annealing effect of IS by examining the ΔV_{th} as a function of time at high temperatures, T > 180 °C. Evidence of this annealing can be seen experimentally using both a DC measurement, where all three components of NBTI are present, and a direct measurement of the IS component, ΔV_{th}(IS), using a pulsed biasing experimental methodology.

II. EXPERIMENT

We have implemented the experimental protocol we developed previously [6] based upon measurements performed using a Keithley Instruments Inc. 4200-SCS Semiconductor Characterization System. To a good approximation, this experimental protocol enables extraction of the different components contributing to the NBTI induced threshold voltage shift, ΔV_{th}. Both NMOS and PMOS devices were produced using a proprietary IBM process on bulk Si wafers with 130 nm channel length by 5 μm channel widths, and 3.4 nm thick oxy-nitide gate insulators were studied in the work presented here. The former NMOS were electrically stressed in accumulation whilst the latter PMOS were stressed in inversion.

To determine the optimum operating conditions for the PMOS/NMOS, the gate to source voltage, V_{gs} was varied from 0 to –1 V (PMOS) or 0 to 1 V (NMOS) whilst measuring the source-drain current, I_{ds}, with a drain to source voltage, V_{ds}, of –50 mV (PMOS) or 50 mV (NMOS). From this we were able to establish the V_{gs}(meas.) at which the maximum of dI_{ds}/dV_{gs} was observed. Subsequently, the unstressed threshold voltage, V_{th}^{o}, was determined using standard techniques [7] and then a

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family of ($I_{ds}(V_{gs})$) curves generated for differing values of V_{th}. Working with a fixed measuring voltage V_{gs}(meas.), equals to the initially determined value yielding the maximum of dI_{ds}/dV_{gs}, the variation in I_{ds} under stress could be translated directly into a ΔV_{th}.

Initial DC stress (recovery) measurements were made in the measure/stress (or recovery)/measure mode with a typical measurement time of ~ 4 μs per source-drain current data point. The ramp time, ~ 20 ns, is that taken to switch the gate bias from some stressing value, V_{gs}(stress), to another value V_{gs}(meas.), at which the source-drain current is measured. The same ramp time was taken to re-establish V_{gs}(stress) following measurement to continue the bias stressing. During V_{gs}(meas.) for the case of the PMOS, the drain to source voltage, V_{ds}, was set to be -50 mV whilst during stressing the bias on the gate, V_{gs}(stress), was chosen to be -3.25 V. The gate-source measurement voltage, V_{gs}(meas.), was typically -0.52 V. For the NMOS case, V_{ds} was 0.05 V, V_{gs}(stress) was -3.5 V whilst V_{gs}(meas.) was 0.5 V. The V_{ds} and V_{gs}(meas.) were chosen to assure the measurement was in the linear regime [7] and the bias stressing conditions for the two types of MOSFETs were chosen to maintain the approximately same gate oxide field [4]. For the DC stressing a nominal stress time of 1500 seconds was applied followed by recovery for the same period of time (a total accumulated time of 3000 seconds).

A second method of stressing involved total AC pulsed stress for 2000 seconds. The pulse repetition frequency was 10 kHz and the duty cycle 10%. During the on time of the pulse (10%) the V_{gs}(stress) was – 3.25 V whilst during the off time of the pulse (90%) it was + 1.5 V. With these pulses, the total actual AC stress time corresponded to 200 seconds and 1800 seconds of relaxation/recovery. The duty cycle was chosen to be 10 % following our earlier study where this was adequate to enable recovery [6] of ΔV_{th}(RC) and ΔV_{th}(FRC) during each pulse. The pulse sequence was arranged so that a point V_{gs}(meas.), I_{ds} was taken immediately following the recovery part of the pulse. Since we are only interested in ΔV_{th}(IS), the recovery voltage, V_{gs}(recov.) was chosen to be 1.5 V in order to assure maximum recovery of ΔV_{th}(RC) and ΔV_{th}(FRC) for both the PMOS and NMOS [6]. This was done for both the DC recovery mode and the pulsed biasing sequence.

III. Results and Discussion

Measurements were carried out over a wide range of temperatures. For the PMOS devices, as a result of DC stress measurements, we observed the simultaneous generation of all three components of ΔV_{th} and after relaxation with positive bias, the only mechanism left to first order is the "permanent" component, ΔV_{th}(IS). As shown in Fig. 1 during the stressing, at T > 180 °C, we observed a "saturation" phenomena in the generation of ΔV_{th}, the total ΔV_{th}(T=200 °C) > ΔV_{th}(T=220 °C). This can be interpreted as evidence for the onset of annealing (reverse reaction) of ΔV_{th}(IS) simultaneously with charged defect creation. Observing the recovery phase (accumulated total time > 1500 s in Fig. 1), there is a general "plateau" trend [3] of ΔV_{th}(IS) as a function of recovery time for T < 180 °C, but it is no longer present for T > 180 °C. This implies that some annealing of IS was occurring simultaneously with IS creation at higher temperatures. Unfortunately, the DC data

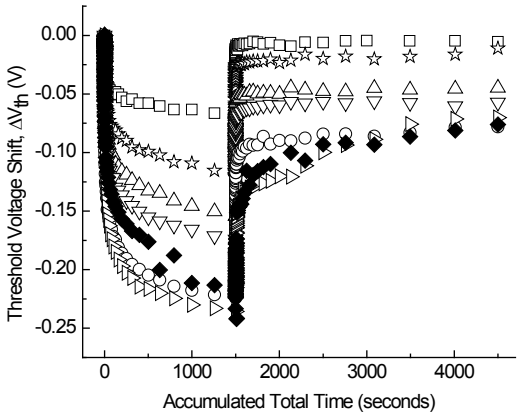

Fig. 1. The threshold voltage shift due to NBTI stress and recovery in a PMOS with V_{gs}(stress) = -3.25 V for 1500 s for multiple temperatures: 50 °C (□), 90 °C (★), 120 °C (△), 150 °C (▽), 180 °C (○), 200° C (▷), and 220 °C (◆).

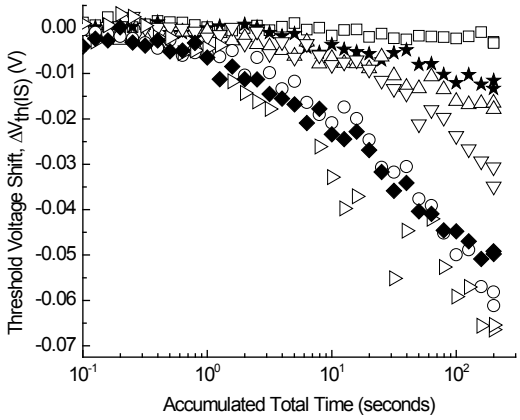

Fig. 2. The measured growth of the interface component of the threshold voltage shift ΔV_{th}(IS) in a PMOS as a function of accumulated total stress time up to 200 seconds is shown for multiple temperatures: 50 °C (□), 90 °C (★), 120 °C (△), 150 °C (▽), 180 °C (○), 200 °C (▷), and 220 °C (◆).

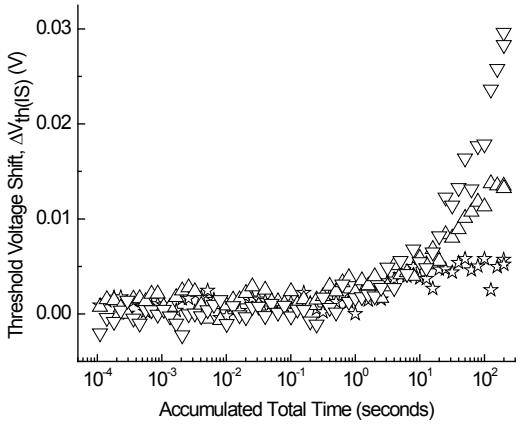

Fig. 3. The measured growth of the interface component of the threshold voltage shift ΔV_{th}(IS) for NMOS as a function of accumulated total stress time up to 200 seconds is shown for multiple temperatures: 90 °C (★), 120 °C (△), and 150 °C (▽).

measures ΔV_{th} for the combined three degradation mechanisms so one can only observe trends and not attribute these to specific components. Data from the AC measurements (Fig. 2) which we argue measure the growth of ΔV_{th}(IS) alone also demonstrated "saturation" during the growth of IS. Based on our data, Figs. 1 and 2, we conclude that the generation of the "permanent" term, ΔV_{th}(IS), is consistent with the presence of a forward reaction term (dominating for T < 180 °C) and a backward reaction (which manifests itself for T > 180 °C) [11]. We have also taken measurements comparing NBTI effects on NMOS devices, that is to say in accumulation. These devices were built using the same technology as for the PMOS devices.

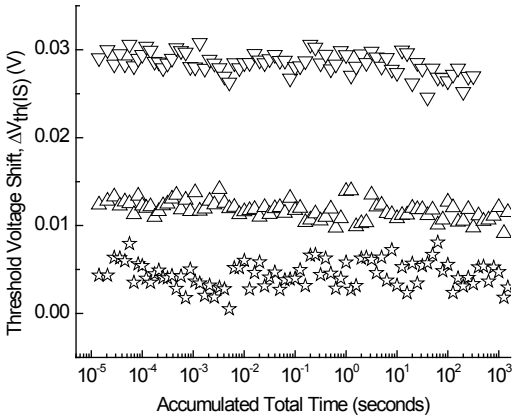

Fig. 4. The measured threshold voltage shift in an NMOS during a recovery bias of V_{gs}(recov.) = 0 V for 1500 s for various temperatures: 90 °C (★), 120 °C (△), and 150 °C (▽).

Again applying AC stress with an on bias stress per pulse of V_{gs}(stress) = – 3.5 V and an off voltage of V_{gs}(recov.) = + 1.5 V we obtain the stress curve shown in Fig. 3 which we attribute solely to ΔV_{th}(IS). The total stress time was again 200 s, as for the PMOS data shown in Fig. 2. In Fig. 4 we show the relaxation data following the AC stress, this relaxation (at 0 V) was continued for 1500 s. To first order we detect no significant annealing in the ΔV_{th}(IS) term.

On the assumption that our methodology enabling extraction of ΔV_{th}(IS) as a function of stress time for PMOS (Fig. 2) and NMOS (Fig.3) is valid, we can compare the growth of ΔV_{th}(IS) in both cases. We arbitrarily take the ln(ΔV_{th}(IS)) for t_{stress} = 100 s, which we plot against the inverse of the absolute temperature. This is shown in Fig. 5. For temperatures < 150 °C the slopes of the lines for PMOS (□) and NMOS (o) are very similar suggesting an activated interface state generation mechanism with an activation energy ~ 0.28 eV. This result is comforting since although the transistor types are different, holes are assumed to be the common tunneling species under negative bias in both cases. Since the interfaces are also expected to be similar at the atomistic level, one would anticipate the NBTI response would also be similar, as observed.

IV. Conclusions

We have studied NBTI in PMOS and NMOS devices at various temperatures. Using a previously defined measurement protocol, we have extracted the threshold voltage variation due

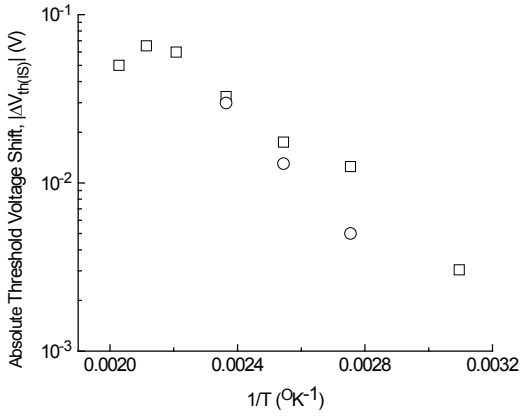

Fig. 5. The absolute threshold voltage shift due to interface states, ΔV_{th}(IS), after 100 s of total accumulated stress at 120 °C with V_{gs} = -3.25 V for PMOS (□) and V_{gs} = -3.50 V for NMOS (○).

to NBTI induced interface states. The activation energy for interface state creation, which we assume is due to hole initiated processes is found to be ~ 0.28 eV in both cases (NMOS and PMOS). Though the exact mechanism by which holes create interface states is unclear, it is assumed to involve hydrogenic species which become protons that can react directly with interfacial Si-H bonds releasing H. Our measurements suggest that for temperatures ≤ 180 °C interface states are created stably, but at or above 180 °C they become unstable and an annealing process, probably involving H or H_2 becomes active. This manifests itself in a reduction in the growth of ΔV_{th}(IS) as a function of stress time as the device temperature is raised.

One can reasonably ask what, if any, are the important consequences of the work reported here? First, we note that there are at least three degradation mechanisms leading to threshold voltage variation as a function of bias temperature stressing as has been suggested by others [12]. There is no reason to assume that these mechanisms have the same activation energy so that one cannot combine them into a generalized form having a unique energy. Secondly, in the case of interface degradation we have demonstrated that there are generation and recovery processes actively dependent upon the temperature at which bias stressing is implemented. Again, no unique activation energy covering both processes can be described. Therefore, the ability to derive predictive reliability models becomes more complex now and must involve not only thermally activated degradation but also recovery.

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